17627

BRAINWARE UNIVERSITY

Term End Examination 2025-2026
Programme – Dip.CSE-2024
Course Name – Digital Electronics
Course Code - DCS30105
(Semester III)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Identify the value of binary 1010 in decimal.

a) 10 b) 12
c) 14 d) 8

(ii) Identify the 2's complement of binary 0101.

a) 1010 b) 1101
c) 1011 d) 1110

(iii) Select the hexadecimal equivalent of binary 1110.

a) E b) F
c) C d) D

(iv) Select the outputs of a half adder.

a) Sum and Carry b) Sum only
c) Carry only d) Difference and Borrow

(v) Select the purpose of a multiplexer.

a) Data distribution b) Data compression
c) Data selection d) Data addition

(vi) Select the number of output lines for a 1-to-4 demultiplexer.

a) 1 b) 2
c) 4 d) 8

(vii) Identify the input condition of JK flip-flop that toggles the output.

a) J=1, K=0 b) J=0, K=1
c) J=0, K=0 d) J=1, K=1

(viii) Identify the input of a D flip-flop.

a) Single data input b) Set and Reset
c) Toggle input d) Clock only

(ix) Identify the condition of output Q in a T flip-flop when input is high.

a) No change | b) Reset
c) Set | d) Toggle

(x) Select the flip-flop with no undefined state.

a) SR flip-flop | b) JK flip-flop
c) D flip-flop | d) T flip-flop

(xi) Identify the type of triggering most commonly used in flip-flops.

a) Level | b) Pulse
c) Edge | d) Delay

(xii) Select the design step that involves choosing flip-flops and logic gates.

a) Excitation table | b) Circuit analysis
c) State assignment | d) Circuit implementation

(xiii) Choose the shift register that can shift both left and right.

a) Serial in Serial out | b) Parallel in Parallel out
c) Universal | d) Right shift

(xiv) Choose the clocking style used in ripple counters.

a) Synchronous | b) Asynchronous
c) Continuous | d) Pulse

(xv) Choose the type of shift register that loads data in parallel.

a) SIPO | b) PIPO
c) SISO | d) SOP

Group-B

(Short Answer Type Questions) 3 x 5=15

2. Describe the concept of Gray code and its purpose. (3)
3. Indicate the difference between Encoder and Priority Encoder. (3)
4. Explain the purpose of the Master-Slave configuration. (3)
5. Differentiate between asynchronous and synchronous inputs in flip-flops. (3)
6. Evaluate the benefits of using ripple counters in digital circuits. (3)

OR

Assess the functionality of a universal shift register. (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Describe the decimal to hexadecimal conversion process with an example. (5)
8. Classify the types of Adders and describe their use cases. (5)
9. Justify the classification of PLA under programmable logic devices. (5)
10. Compare Master-Slave Flip-Flops with Edge Triggered Flip-Flops in terms of behavior. (5)
11. Justify the use of universal shift registers in microprocessor systems. (5)
12. Contrast the state transition diagram for a 2-bit binary counter using T Flip-Flops. (5)

OR

Evaluate the impact of race-around conditions in level-triggered JK Flip-Flops. (5)

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