17642

BRAINWARE UNIVERSITY

Term End Examination 2025-2026
Programme – Dip.RA-2024
Course Name – Digital Electronics
Course Code - DEC30103
(Semester III)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Identify what is the decimal equivalent of the binary number 11011011

a) 219 b) 217
c) 211 d) 128

(ii) Which of following are identified as universal gates

a) NAND & NOR b) AND & OR
c) XOR & XNOR d) None of these

(iii) The fastest logic in logic families is indicated as

a) ECL b) TTL
c) CMOS d) LSI

(iv) Identify how many NAND gates required to implement NOT gate?

a) 1 b) 2
c) 3 d) 4

(v) Calculate minimum number of two input NAND gates required to realize XOR gate is

a) 3 b) 4
c) 5 d) 6

(vi) The gates required to develop a half adder are

a) EX-OR gate and NOR gate b) EX-OR gate and OR gate
c) EX-ORgate and AND gate d) Four NAND gates.

(vii) Karnaugh map is chosen for the purpose of-

a) Reducing the electronic circuits used b) To map the given Boolean logic function
c) To minimize the terms in a Boolean expression d) To maximize the terms of a given a Boolean expression

(viii) In a 3-variable Karnaugh Map, determine how many cells are there?

a) 4 b) 8

c) 16 d) 32

(ix) Determine the select lines of 16 to 1 multiplexer

a) 4 b) 3
c) 5 d) 1

(x) Determine the output: A +AB+ABC+ABCD+ABCDE+....

a) 1 b) A
c) A + AB d) AB

(xi) A binary-to-octal decoder is constructed through

a) 3-line to 8-line decoder b) 1-line to 8-line decoder
c) 4-line to 8-line decoder d) any lines to 8-line decoder

(xii) A 32:1 mux can be constructed using

a) two 16:1 muxs and one two input OR gate b) two 16:1 muxs and one two input AND gate
c) two 16:1 muxs and two two input OR gate d) two 16:1 muxs only

(xiii) Identify how many NAND gates required to implement a OR gate-

a) 1 b) 2
c) 3 d) 4

(xiv) The expression Y=AB+BC+AC shows

a) EX-OR operation b) SOP operation
c) POS operation d) NOR operation

(xv) Through a NOT gate, a D flip-flop can be constructed from

a) S-R flip flop b) J-K flip flop
c) S-K flip flop d) T flip flop

Group-B

(Short Answer Type Questions) 3 x 5=15

2. Describe EXOR gate with its Boolean expression, truth table and logical symbol. (3)

3. Apply K-map to simplify the following expression: (3)
Y (A, B, C, D) = Σ m (1, 3, 4, 5,6,7,9,11,12,13,14,15)

4. Explain SOP and POS. (3)

5. Explain D flip-flop with its truth table, circuit diagram and working principle. (3)

6. Construct full adder circuit by using logic gates. (3)

OR

Construct full subtractor circuit by using logic gates. (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Describe NAND gate and demonstrate the action of NAND gate as Universal gate. (5)

8. Explain the construction of half adder using NAND gate and NOR gate. (5)

9. Explain 4:1 Multiplexer through block diagram, truth table, logical expression and circuit diagram. (5)

10. Explain S-R flip-flop with present state-next state table, excitation table and logical expression of next state output (5)

11. Explain the construction of J-K flip flop using D flip flop (5)

12. Construct 4:1 Multiplexer using three 2:1 Multiplexer. (5)

OR

Design a full adder circuit using a 3 to 8 line decoder. (5)

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