18137

BRAINWARE UNIVERSITY

Term End Examination 2025-2026
Programme – B.Tech.(EE)-2024
Course Name – Digital Electronics
Course Code - BTE30103
(Semester III)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A
(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Select which type of counter easily produced a series of equal space time pulses :
a) Johnson shift b) Clock shift
c) Binary shift d) Ring counter

(ii) Recall the three output conditions of 3- state buffer are:
a) High Impedance, 0, float b) Negative, positive, 0
c) Low Impedance, float d) High, Low, float

(iii) Select the equivalent octal number of the decimal number 153
a) 231 b) 251
c) 241 d) 261

(iv) Identify which one of the following is correct for full adders
a) Full adders have the capability of directly adding decimal numbers(
b) Full adders are used to make half adders
c) Full adders are limited to two inputs since there are only two binary digits
d) In a parallel full adder, the first stage may be a half adder

(v) Choose the number of inputs required for a half-subtractor
a) 1 b) 2
c) 3 d) 4

(vi) Choose the output of an odd parity checker for the input bits: 10101
a) 1 b) 0
c) Undefined d) Error

(vii) Select the group of 1s in 4 cells of a K – map called
a) Pair b) Quad
c) Octet d) Octave

(viii) Choose the frequency of the output from a JK flip – flop, when J = 1, K = 1, and a clock with pulse waveform is given

a) Half the frequency of clock input
b) Equal to the frequency of clock input
c) Twice the frequency of clock input
d) Independent of the frequency of clock input

(ix) Select the number of bits are needed to store one BCD digit

a) 2 bits
b) 4 bits
c) 3 bits
d) 1 bit

(x) Identify the output if an input signal 1 is applied to a NOT gate

a) 0
b) 1
c) Either 0 & 1
d) None of these

(xi) Select the fixed-point representation of the decimal number 6.125 in an 8-bit system (assuming 4 bits for integer and 4 bits for fraction).

a) 0110.1100
b) 0110.0010
c) 0110.0110
d) 0110.1010

(xii) Choose the type of RAM that needs to be refreshed periodically.

a) SRAM.
b) DRAM.
c) ROM.
d) Cache.

(xiii) Determine which memory is typically used for cache.

a) SRAM.
b) DRAM.
c) ROM.
d) EEPROM.

(xiv) Choose the reason why DRAM is preferred for main memory.

a) Faster than SRAM.
b) Less expensive and higher capacity.
c) Non-volatile.
d) Requires less refreshing.

(xv) Identify the dual of the Boolean expression A+(B·C)

a) A·(B+C)
b) A+B+C
c) A·B·C
d) None of these

Group-B

(Short Answer Type Questions) 3 x 5=15

2. State the binary equivalent of the Hexadecimal number 2FA. (3)
3. Explain the working principle of priority encoder. (3)

4. Describe EXNOR gate with its Boolean expression, truth table and logical symbol. (3)

5. Explain 2:4 Decoder through block diagram, truth table and logical expression. (3)

6. Explain SIPO register. (3)

OR

Explain half adder with its block diagram, truth table and circuit diagram by using logic gates. (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Recall the significance of BCD codes. (5)

8. Examine and Minimize the following boolean function- $F(A, B, C, D) = \Sigma m(0, 1, 3, 5, 7, 8, 9, 11, 13, 15)$ (5)

9. Differentiate between Sequential and Combinational circuits. (5)

10. Illustrate Full-Adder using suitable diagram. (5)

11. Construct 8:1 multiplexer using 4:1 multiplexer and OR gate. (5)

12. Differentiate Static RAM (SRAM) and Dynamic RAM (DRAM) in terms of structure and functionality. (5)

OR

Explain the working of Flash type ADC. (5)

****