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# BRAINWARE UNIVERSITY

**Term End Examination 2025-2026**
**Programme – Dip.EE-2024**
**Course Name – Digital Electronics**
**Course Code - DEE30103**
**( Semester III )**



**Full Marks : 60** **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

**Group-A**

(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Select the binary equivalent of the decimal number 368

a) 101110000 b) 110110000
c) 111010000 d) 111100000

(ii) Select the decimal equivalent of Binary number 10101

a) 25 b) 21
c) 37 d) 31

(iii) Select the gate that can be used as controlled inverter

a) AND b) OR
c) NAND d) XOR

(iv) Select the correct answer -In K-Map, individual cells are observed as

a) Binary code b) Grey Code
c) BCD Code d) None of these

(v) Identify which one of the following is a major difference between a half adder and a full adder

a) Full-adders are made up of two half-adders b) Full adders can handle double-digit numbers
c) Full adders have a carry input capability d) Half adders can handle only single-digit numbers

(vi) Choose digital logic circuits can be used to add more than 1 – bit simultaneously

a) Full – adder b) Ripple – carry adder
c) Half – adder d) Serial adder

(vii) Choose the gate combination used for the Borrow output in a half-subtractor

a) AND and NOT gates b) OR and XOR gates
c) NAND and NOR gates d) XOR and AND gates

(viii) Choose the output from a D flip-flop if D = 1 and the clock is low

a) No change
b) Toggle between 0 and 1
c) 0
d) 1

(ix) Select the group of 1s in 4 cells of a K – map called

a) Pair
b) Quad
c) Octet
d) Octave

(x) Choose the frequency of the output from a JK flip – flop, when J = 1, K = 1, and a clock with pulse waveform is given

a) Half the frequency of clock input
b) Equal to the frequency of clock input
c) Twice the frequency of clock input
d) Independent of the frequency of clock input

(xi) Identify the output of a demultiplexer when the select lines are set to a specific binary value.

a) All outputs are activated.
b) Only the corresponding output line is activated.
c) The output is always high.
d) The output depends on the enable signal only.

(xii) Select the correct option-On addition of -46 and +28 using 2's complement, we get _____________

a) -10010
b) -00101
c) 01011
d) 0100101

(xiii) Determine which component is used to store a single bit of data.

a) Latch.
b) Counter.
c) Register.
d) Decoder.

(xiv) Determine which type of counter has all flip-flops triggered simultaneously.

a) Asynchronous counter.
b) Ring counter.
c) Synchronous counter.
d) Johnson counter.

(xv) Determine which memory is typically used for cache.

a) SRAM.
b) DRAM.
c) ROM.
d) EEPROM.



## Group-B

(Short Answer Type Questions) 3 x 5=15

2. Examine each pair of decimal numbers to binary and add using the 2's complement form: (3)
3. Explain 2:4 Decoder through block diagram, truth table and logical expression. (3)
4. Construct Ex-OR gate using NAND gates only. (3)
5. Explain the differences between static RAM and dynamic RAM. (3)
6. Explain SISO register. (3)

**OR**

Explain SIPO register. (3)

## Group-C

(Long Answer Type Questions) 5 x 6=30

7. Explain Commutative law, Associative law related to Boolean algebra with example. (5)
8. Examine and Minimize the following boolean function- F(A, B, C, D) = Σm(0, 1, 3, 5, 7, 8, 9, 11, 13, 15) (5)
9. State the technique of converting Gray to binary code and express 1001 in Binary code. (5)

10. Design a two bit flash type Analog to Digital converter and explain its working. (5)
11. Explain the construction of full adder circuit using two half adder through a block diagram. (5)

12. Construct 4:1 Multiplexer using 2:1 Multiplexer and one OR gate. (5)

**OR**

Construct 8:1 multiplexer using 4:1 multiplexer and OR gate. (5)

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