15106

BRAINWARE UNIVERSITY

Term End Examination 2025-2026
Programme – B.Tech.(EE)-2023
Course Name – Computer Organization & Architecture
Course Code - OE-EE501C
(Semester V)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Identify The main virtue for using single Bus structure is ____________

a) Fast data transfers
b) Cost effective connectivity and speed
c) Cost effective connectivity and ease of attaching peripheral devices
d) None of the mentioned

(ii) Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. Select the option for the execution of the same instruction that processor do it faster.

a) A
b) B
c) Both take the same time
d) Insufficient information

(iii) Select the register that is initialized first during the execution of a program.

a) MDR
b) IR
c) PC
d) MAR

(iv) Identify The registers, ALU and the interconnection between them are collectively called as _____

a) process route
b) information trail
c) information path
d) data path

(v) Choose that In a normal adder circuit, the delay obtained in a generation of the output is _______

a) 2n + 2
b) 2n
c) n + 2
d) None of the mentioned

(vi) Identify the product of -13 & 11 is ______________

a) 1100110011
b) 1101110001
c) 1010101010
d) 1111111000

(vii) Select the correct option that A control bit called ________ has to be provided to each block in set-associative.

a) Idol bit
b) Valid bit
c) Reference bit
d) All of the mentioned

(viii) Select the correct option:In LRU, the referenced blocks counter is set to'0' and that of the previous blocks are incremented by one and others remain same, in the case of ______

a) Hit
b) Miss
c) Delay
d) None of the mentioned

(ix) Select that the binary address issued to data or instructions are called as ______

a) Physical address
b) Location
c) Relocatable address
d) Logical address

(x) Select that the contents of the EPROM are erased by ________

a) Overcharging the chip
b) Exposing the chip to UV rays
c) Exposing the chip to IR rays
d) Discharging the Chip

(xi) Choose The computer architecture that aimed to reduce the time of execution of instructions.

a) CISC
b) RISC
c) ISA
d) ANNA

(xii) Select the correct answer about the end instruction.

a) It ends the generation of a signal
b) It ends the complete generation process
c) It starts a new instruction fetch cycle and resets the counter
d) It is used to shift the control to the processor

(xiii) Choose the architecture that emphasizes simple instructions and single clock cycle execution

a) CISC
b) DSP
c) RISC
d) None of the mentioned

(xiv) Select the correct option : To overcome the lag in the operating speeds of the I/O device and the processor we use ___________

a) BUffer spaces
b) Status flags
c) Interrupt signals
d) Exceptions

(xv) Select in DMA transfers, the required signals and addresses are given by the ___________

a) Processor
b) Device drivers
c) DMA controllers
d) The program itself

Group-B

(Short Answer Type Questions) 3 x 5=15

2. Describe cache memory in brief. (3)
3. Classify the different types of addressing Modes. (3)
4. Compute the principle of operation of a carry look-ahead adder. (3)
5. Classify the different types of registers. (3)
6. An Address space is specified by 24 bits and corresponding memory space by 16bits. Conclude How many words are there in a) virtual memory b) Main memory (3)

OR

Explain the role of MAR and MDR. (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time of 250 ps and a CPI of 2.0 for some program, and computer B has a clock cycle time of 500 ps and a CPI of 1.2 for the same program. predict Which computer is faster for this program and by how much? (5)

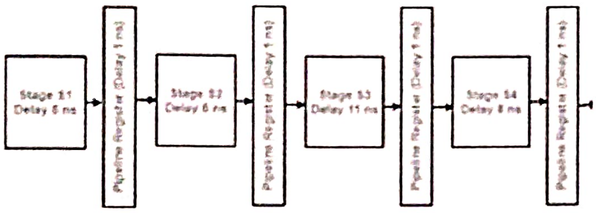
8. Illustrate and Draw the full adder circuit and give the truth table. (5)

9. Consider a fully associative mapped cache with block size 4 KB. The size of main memory is 16 GB. Solve and Find the number of bits in tag. (5)

10. (5)

Consider an instruction pipeline with four stages (S1, S2, S3 and S4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure-

Determine the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?



11. Discuss the principle behind Booth's multiplier. Write the advantage of using Booth algorithm. (5)

12. Classify the five stages of Instruction Executions. (5)

OR

Contrast the difference between RISC and CISC. (5)

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