BRAINWARE UNIVERSITY

Term End Examination 2022
Programme – B.Sc.(ANCS)-Hons-2019/B.Sc.(ANCS)-Hons-2020/B.Sc.(ANCS)-Hons-2021/B.Sc.(ANCS)-Hons-2022
Course Name – Electronics
Course Code - GEEC101
(Semester I)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 30=30

1. *Choose the correct alternative from the following :*

(i) Select the binary equivalent of the decimal number 368

a) 101110000 b) 110110000
c) 111010000 d) 111100000

(ii) Select the decimal equivalent of hex number 1A53

a) 6793 b) 6739
c) 6973 d) 6379

(iii) To design a non-inverting adder inputs are applied

a) Non-inverting terminal b) Inverting terminal
c) Both inverting and non-inverting terminal d) None of these

(iv) Find the decimal equivalent number of hexadecimal number 'A0'

a) 80 b) 256
c) 100 d) 160

(v) During reverse bias, a small current develops which is known as

a) Forward current b) Reverse current
c) Reverse saturation current d) Active current

(vi) Flip-flops can be used to design

a) latches b) bounce –elimination switches
c) registers d) all of the above

(vii) Find the 2's complement of the number 1101101 -

a) 0101110 b) 0111110
c) 0110010 d) 0010011

(viii) When an input signal A=11001 is applied to a NOT gate serially, its output signal is represented as

a) 00111
b) 00110
c) 10101
d) 11001

(ix) An operational amplifier possesses

a) Very large input resistance and very large output resistance
b) Very large input resistance and very small output resistance
c) Very small input resistance and very small output resistance
d) Very small input resistance and very large output resistance.

(x) Convert decimal 153 to octal. Equivalent in octal will be

a) $(231)_8$
b) $(331)_8$
c) $(431)_8$
d) none of these

(xi) What is the left hand section of a junction transistor called?

a) base
b) Collector
c) depletion region
d) Emitter

(xii) The simplified form of Boolean expression $\overline{A}+A\overline{B}$ is

a) A+B
b) $A+\overline{B}$
c) $\overline{A}+\overline{B}$
d) none of these

(xiii) The fastest logic in logic families is indicated as

a) ECL
b) TTL
c) CMOS
d) LSI

(xiv) Consider the inverting OP-AMP with R1 (input resistance) =1k ohm ,R2 (feedback resistance) =50k ohm and power supply voltages ±12V. Find the output voltage for an input voltage 1V.

a) -50V
b) -12V
c) 50V
d) 12V

(xv) Calculate how many AND gates are required to realize Y = CD+EF+G

a) 4
b) 5
c) 3
d) 2

(xvi) Calculate how many two input AND gates and two input OR gates are required to realize
Y = BD+CE+AB

a) 1,1
b) 4,2
c) 3,2
d) 2,3

(xvii) In the operation of an NPN transistor, the electrons cross which region?

a) emitter region
b) The region where there is high depletion
c) the region where there is low depletion
d) P type base region

(xviii) The device which changes from serial data to parallel data is

a) counter
b) multiplexer
c) demultiplexer
d) flip-flop

(xix) Select the two inputs of The NOR gate when output will be high

a) 00
b) 10
c) 01
d) 11

(xx) When does the transistor act like an open switch?

a) cut off region
b) Active region
c) saturated region
d) None of these

(xxi) The gates required to develop a half adder are

a) EX-OR gate and NOR gate
b) EX-OR gate and OR gate
c) EX-OR gate and AND gate
d) Four NAND gates.

(xxii) According to the property of minterm, calculate how many combination will have value equal to 1 for K input variables?

a) 0
b) 1
c) 2
d) 3

(xxiii) The output of a certain op-amp circuit changes by 20 V in 4 μs. Calculate slew rate

a) 50 V/μs
b) 500 mV/μs
c) 5 V/μs
d) 500 V/μs

(xxiv) Choose the following combinations of logic gates can decode binary 1101?

a) One 4-input AND gate
b) One 4-input AND gate, one inverter
c) One 4-input AND gate, one OR gate
d) One 4-input NAND gate, one inverter

(xxv) Which of the following circuits consider under the class of sequential logic circuits?

1. Full adder
2. Full subtractor
3. Half adder
4. J-K flip
5. Counter

a) 1 and 2
b) 2 and 3
c) 3 and 4
d) 4 and 5

(xxvi) Which of the following circuits consider under the class of combinational logic circuits?

1. Full adder
2. Full subtractor
3. Half adder
4. J-K flip
5. Counter

a) 1 only
b) 3 and 4
c) 4 and 5
d) 1,2 and 3

(xxvii) Evaluate the required number of half adders to add two m-bit numbers

a) 2m – 1
b) $2^m - 1$
c) 2m + 1
d) 2m

(xxviii) Choose a logic circuit that accepts several data inputs and allows only one of them at a time to get through to the output

a) multiplexer
b) demultiplexer
c) transmitter
d) receiver

(xxix) The output Q_n of a J-K flip-flop is 1. it changes to 0 when a clock pulse is applied. the input J_n and K_n are evaluated as

a) 0 and X
b) 1 and X
c) X and 1
d) X and 0

(xxx) Select the two inputs of the NAND gate if the output is low

a) 00
b) 01
c) 10
d) 11

Group-B

(Multiple Choice Type Question) 3 x 10=30

2. *Choose the correct alternative from the following :*

(i) To design the 4:1 MUX how many minimum basic gates are required

a) 1 NOT gates, 3 AND gates
b) 2 NOT gates, 3 AND gates
c) 1 NOT gates, 4 AND gates
d) 2 NOT gates, 4 AND gates

(ii) When an inventer is placed between the inputs of an S-R flip-flop for creating a new flip-flop which is known as

a) J-K flip-flop
b) master-slave flip-flop
c) T flip-flop
d) D flip-flop

(iii) Choose the correct option: how many gates are required to implement Y=AB +BC

a) 2 AND gates and 2 OR gate
b) 2 AND gates and 1 OR gate
c) 1 AND gates and 1 OR gate
d) 1 AND gates and 2 OR gate

(iv) Choose the correct option: how many gates are required to implement a full adder

a) 9 NAND gates
b) 8 NAND gates
c) 9 AND gates
d) 8 AND gates

(v) Calculate the octal to hexadecimal: $(1257.625)_8 = (?)_{16}$

a) 2AE.CB8
b) 2AF.CB8
c) 2AF.CA8
d) 2AE.CA8

(vi) A certain OP-amp has bias currents of 50 μA and 49.3 μA . The input offset current is_____.

a) 700 nA
b) 99.3 μA
c) 7 nA
d) None of these

(vii) To evaluate Y=

$$\bar{A}B\bar{C}+\bar{A}\bar{B}C+\bar{A}BC+A\bar{B}C$$

a) $Y = \bar{A}B + \bar{B}C$
b) $Y = \bar{A}B + \bar{B}$
c) $Y = \bar{A}B + C$
d) None of these

(viii) To solve the $(1983.5625)_{10} = (?)_{16}$

a) 7BF.9
b) 7BE.A
c) 7BF.8
d) None of these

(ix) Convert a 16:1 MUX using 4:1 MUX only. How many 4:1 MUX is required

a) 3
b) 4
c) 5
d) 6

(x) What is 1's complement and 2's of a number?

a) 1's complement, one convert to zero and zero convert to one. 2's complement = 1's +1
b) 1's complement, one convert to zero and zero convert to one. 2's complement = 1's - 1
c) 1's complement, one convert to zero and zero convert to one. 2's complement = 1's * 1
d) None of these

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