BRAINWARE UNIVERSITY

Term End Examination 2022
Programme – B.Tech.(ECE)-2019/B.Tech.(ECE)-2020
Course Name – Computer Architecture
Course Code - PCC-EC502
(Semester V)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A
(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Select what a stack is

a) an 8-bit register in the microprocessor
b) an 16-bit register in the microprocessor
c) a set of memory locations in R/WM reserved for storing information temporary during the execution of computer
d) a 16-bit memory address stored in the program counter

(ii) Convert the binary number (1111000011110000) to hexadecimal number

a) 1010
b) F0F0
c) 7070
d) 5050

(iii) Identify when a program that translates a high-level language program into machine language program line-by-line is called

a) Compiler
b) Interpreter
c) Assembler
d) Debugger

(iv) Tell that two input NOR gate gives logic high output only when

a) one input is high
b) one input is low
c) Both inputs are low
d) Both inputs are high

(v) Identify binary subtraction is performed In a digital computer

a) in the same way as we perform subtraction in decimal number
b) Using 2's complement method
c) Using 9's complement method
d) Using 10's complement method

(vi) Write both CLA and CPA are kind of

a) Serial Adder
b) Parallel Adder
c) Special type of adder
d) None of these

(vii) Select from the below that the addition is done with the help of_____ in ALU

a) Adder
b) Subtractor
c) Multiplier
d) By program only

(viii) Select from the below if a multiplexer has 16 input lines, then how many select lines it will has

a) 2
b) 4

c) 6 d) 8

(ix) Calculate if there are multiple inputs are there and only one input will be selected at a time as output, then which of the following circuit will be used?

a) Multiplexer b) Decoder
c) Encoder d) Any gate

(x) Select the last memory size if FFFF be the last memory location

a) 1K b) 16K
c) 32K d) 64K

(xi) Select from below what is it called when the average time required to reach a storage location in memory and obtain its contents

a) seek time b) turaround time
c) access time d) transfer time

(xii) Decide that the Cache memory works on the principle of

a) Locality of data b) Locality of reference
c) Both option a and b d) None of these

(xiii) Select what type of Von Neumann architecture is

a) SISD b) SIMD
c) MISD d) MIMD

(xiv) Write how many address lines are needed to address each memory locations in a 2048 x 4 memory chip?

a) 8 b) 10
c) 11 d) 12

(xv) Write which one is better

a) Pipelined processor b) VLIW processor
c) Super-pipelined processor d) Both (VLIW processor) and (Super-pipelined processor)

Group-B

(Short Answer Type Questions) 3 x 5=15

2. Write about different types of hazards in pipeline architecture (3)
3. Explain the fixed and floating point representation of numbers (3)
4. Illustrate difference between Write back and Write through policy (3)
5. Describe the LRU page replacement algorithm with example. (3)
6. Write about different types of interrupts (3)

OR

Explain software interrupts (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Tell the types of pipelining hazards (5)
8. Calculate the page fault for the reference string 3,2,1,0,3,2,4,3,2,1,0,4 with 3 page frames using FIFO and optimal page replacement algorithm. (5)
9. Explain the memory hierarchy with diagram (5)
10. Write about different stages of an instruction cycle (5)
11. Test the page fault for the reference string 7,0,1,2,0,3,0,4,2,3,0,2,3,2,3 with 3 & 4 page frames using Least recently used page replacement algorithm (5)
12. Illustrate Direct memory access (DMA) (5)

OR

Explain Carry look ahead adder with diagram (5)

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