



BRAINWARE UNIVERSITY

Term End Examination 2022
Programme – B.Tech.(CSE)-2019
Course Name – VLSI
Course Code - OEC-701D
(Semester VII)

Full Marks : 60 Time : 2:30 Hours

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 15=15 1. Choose the correct alternative from the following: (i) VLSI technology identifies ______ to form integrated circuit. a) Transistors b) switches d) buffers c) diodes (ii) Large-scale integration is defined by _____ number of transistors. a) 10 to 500 b) 1 to 10 c) 20,000 to 1,000,000 d) 500 to 20,000 (iii) Choose, P-well doping concentration and depth will affect the _____ a) threshold voltage b) Vss c) Vdd d) Vgs (iv) State in which method regularity is used to reduce complexity. b) hierarchical approach a) random approach c) algorithmic approach d) semi-design approach (v) Write the basic chemical reaction used for epitaxial growth of pure silicon. b) oxygen reduction of silicon tetrachloride. a) hydrogen reduction of silicon tetrachloride. c) hydrogen reduction of silicon d) oxygen reduction of silicon pentachloride. pentachloride. (vi) Complete: In depletion mode, source and drain are connected by a) insulating channel b) conducting channel

(viii) Express, in diffusion process of nMOS, impurity is desired.

(vii) Cite that the photoresist layer is exposed to

(ix) Identify, if Sllicon-di-oxide is a good insulator.

a) Visible light

a) n type

c) np type

a) correct

c) sometimes

c) Infra red light

d) Vss

d) LED

b) p type

d) never

b) not correct

b) Ultraviolet light

d) none of the mentioned

(x)	Conclude The drain current is varied by:			
	a) Gate to source voltage	b) Gate current		
	c) Source Voltage	d) None of the mentioned		
(xi)	xi) Deduce the logical low voltage (logic 0) or negative voltage on the gate of p-MOSFET			
	forms			
	a) Channel of negative carriers	b) Channel is not formed		
	c) Channel is clipped	d) Channel of positive carriers		
(xii)	(xii) Choose, which MOSFET is generally connected to the Vdd in a circuit?			
	a) PMOS	b) NMOS		
	c) CMOS	d) DMOS		
(xiii)	(xiii) Conclude, the current through the n-MOS transistor will flow when:			
	a) Vgs > Vtreshold, Vds=0	b) Vgd < Vtreshold, Vds=0		
	c) Vgs > Vtreshold, Vds>0	d) Vgd > Vtreshold, Vds<0		
(xiv) Report the switching threshold voltage VTH for an ideal inverter is equal to:				
	a) (VDD-VOL)/2	b) VDD		
	c) (VDD)/2	d) 0		
(xv)	(xv) Report the electrical equivalent component for MOS structure is:			
	a) Resistor	b) Capacitor		
	c) Inductor	d) Switch		
Group-B				
(Short Answer Type Questions) 3 x 5=15				
	. 6		(5)	
	eport functions of SiO2.		(3)	
3. Examine Vapor Phase Epitaxy.4. With circuit diagram of CMOS NAND gate, describe output formation of the truth table, for			(3) or (3)	
each input combination.				
·			(3)	
6. Construct CMOS full adder by any two different ways.			(3)	
OR			(-)	
R	ewrite Full custom and Semi-custom design.		(3)	
Group-C				
	(Long Answer Ty	pe Questions)	5 x 6=30	
7. Identify Analog & Digital VLSI chips, General purpose, ASIC, PLA and FPGA.			(5)	
8. Illustrate Ion Implantation.			(5)	
9. Construct the diagrams for every step in CMOS fabrication.			(5)	
10. Illustrate Stick diagram.11. Analyze the drawing of 3-input CMOS NAND & NOR Gates and their truth tables with			(5)	
11. Analyze the drawing of 3-input CMOS NAND & NOR Gates and their truth tables with explanation of how each output is generated. (5)			(5)	
12. Criticize Full custom and Semi-custom design.			(5)	
	OF	R	(- /	
	ustify FPGA building block architectures.		(5)	
