



- (x) Conclude The drain current is varied by:
  - a) Gate to source voltage
  - b) Gate current
  - c) Source Voltage
  - d) None of the mentioned
- (xi) Deduce the logical low voltage (logic 0) or negative voltage on the gate of p-MOSFET forms \_\_\_\_\_
  - a) Channel of negative carriers
  - b) Channel is not formed
  - c) Channel is clipped
  - d) Channel of positive carriers
- (xii) Choose, which MOSFET is generally connected to the Vdd in a circuit?
  - a) PMOS
  - b) NMOS
  - c) CMOS
  - d) DMOS
- (xiii) Conclude, the current through the n-MOS transistor will flow when:
  - a)  $V_{gs} > V_{treshold}$ ,  $V_{ds}=0$
  - b)  $V_{gd} < V_{treshold}$ ,  $V_{ds}=0$
  - c)  $V_{gs} > V_{treshold}$ ,  $V_{ds}>0$
  - d)  $V_{gd} > V_{treshold}$ ,  $V_{ds}<0$
- (xiv) Report the switching threshold voltage  $V_{TH}$  for an ideal inverter is equal to:
  - a)  $(V_{DD}-V_{OL})/2$
  - b)  $V_{DD}$
  - c)  $(V_{DD})/2$
  - d) 0
- (xv) Report the electrical equivalent component for MOS structure is:
  - a) Resistor
  - b) Capacitor
  - c) Inductor
  - d) Switch

**Group-B**

(Short Answer Type Questions)

3 x 5=15

- 2. Report functions of SiO<sub>2</sub>. (3)
- 3. Examine Vapor Phase Epitaxy. (3)
- 4. With circuit diagram of CMOS NAND gate, describe output formation of the truth table, for each input combination. (3)
- 5. What are the different types of VLSI Chips? (3)
- 6. Construct CMOS full adder by any two different ways. (3)

**OR**

- Rewrite Full custom and Semi-custom design. (3)

**Group-C**

(Long Answer Type Questions)

5 x 6=30

- 7. Identify Analog & Digital VLSI chips, General purpose, ASIC, PLA and FPGA. (5)
- 8. Illustrate Ion Implantation. (5)
- 9. Construct the diagrams for every step in CMOS fabrication. (5)
- 10. Illustrate Stick diagram. (5)
- 11. Analyze the drawing of 3-input CMOS NAND & NOR Gates and their truth tables with explanation of how each output is generated. (5)
- 12. Criticize Full custom and Semi-custom design. (5)

**OR**

- Justify FPGA building block architectures. (5)

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