BRAINWARE UNIVERSITY

Term End Examination 2021 - 22

Programme – Bachelor of Technology in Computer Science & Engineering

Course Name – Advanced Computer Architecture

Course Code - PEC-702B

(Semester VII)

Time : 1 Hr.25 Min. **Full Marks : 70**

[The figure in the margin indicates full marks.]

Group-A

(Multiple Choice Type Question) 1 x 70=70

Choose the correct alternative from the following :

(1) Number of instructions is less in

a) Scaler Program
b) Vector Program
c) It cannot be said
d) Equal in both scalar and vector.

(2) Which of the following is the first field in vector instruction format?

a) Base Address
b) Address Offset
c) Operation Code
d) Length

(3) Starting address is also known as

a) Address offset
b) Base address
c) Displacement
d) None of the above

(4) A compiler that converts a scalar instruction into corresponding vector instruction is kn own as

a) DSP
b) Analog Compiler
c) GCC Compiler
d) Vectorising Compiler

(5) Which of the following processor is a vector processor?

a) BSP
b) ILLIAC-IV
c) PEPE
d) TI-ASC

(6) Vector Squire Root is an example of _____ operation

a) Unary
b) Binary
c) Ternary
d) All of the above types

(7) Vector Stride value is used to access_____ vectors.

a) One dimensional
b) Two dimensional
c) Three dimensional
d) Multidimensional

(8) If UVL = 100 and MVL = 32, then the loop will be iterated

a) One time
b) Two time
c) Three time
d) Four time

(9) If a vector has 10 X 10 = 100 elements in row-major fashion, then to access the elemen ts according to column will be

a) 1
b) 2
c) 5
d) 10

(10) Addition is the responsibility of

a) ALU
b) CU
c) Register Set
d) None of the above

(11) In an instruction format, first block will be always a

a) Operand
b) Operand Address
c) Addressing Mode
d) Op-Code

(12) ILLIAC-IV is a

a) Multiprocessor
b) Vector processor
c) Array processor
d) Super computer

(13) Which one stores the starting address of program?

a) PC
b) SP
c) AC
d) DR

(14) Which bus is bidirectional?

a) Address
b) Data
c) Control
d) All of these

(15) Which uses shared memory?

a) UMA
b) NUMA
c) COMA
d) None of these

(16) Which of the following is not a data hazard?

a) RAR
b) RAW
c) WAR
d) WAW

(17) Which particular stage in instruction cycle is used by ALU?

a) IF
b) ID
c) OF
d) EX

(18) The product of time and stage in case of linear pipeline is

a) Space-Time Diagram
b) Time-Space Diagram
c) Time-Space Span
d) Space-Time Span

(19) In which stage, addressing mode will be fin out?

a) IF
b) ID
c) OF
d) EX

(20) Which one is not a data hazard?

a) RAR
b) RAW
c) WAR
d) WAW

(21) Which one is not a type of internal forwarding

a) Store – fetch forwarding
b) Fetch – fetch forwarding
c) Store –store overwriting
d) Store –store forwarding

(22) Which of the following has multiple output?

a) Linear pipelining
b) General pipelining
c) NOT Gate
d) None of these

(23) Which one is the representation of data flow in general pipeline processor?
a) Space-Time diagram
b) Gantt Chart
c) Reservation Table
d) Pie Chart

(24) User view of memory is only possible in
a) Paging
b) Segmentation
c) Segmentation with paging
d) Some other Scheme

(25) Equal size partitions are applicable in
a) Paging
b) Segmentation
c) Segmentation with paging
d) Any other scheme

(26) Which one is not a state of switch box?
a) Straight
b) Exchange
c) Upper Broadcast
d) Sigmoid

(27) Which one is a sequential circuit?
a) Flip-flop
b) AND Gate
c) NAND Gate
d) Decoder

(28) What is the Hex equivalent of the binary number 11111111
a) 11
b) 22
c) DD
d) FF

(29) Which of the following is a message passing system?
a) Cray-I
b) Transputer
c) Cray - II
d) C.m*

(30) Which one takes the top position in memory hierarchy?
a) Cache
b) Main memory
c) Registers
d) HDD

(31) Which one is not present inside of a CPU?
a) ALU
b) CU
c) Register
d) Key

(32) Which one is not an input device?
a) Mouse
b) Keyboard
c) Scanner
d) Printer

(33) Which of the following is the universal gate?
a) AND
b) OR
c) NOR
d) XOR

(34) Only one output is supported by
a) AND gate
b) OR gate
c) NOT gate
d) NAND gate

(35) If a multiplexer has 16 input lines, then how many select lines it will has?
a) 2
b) 4
c) 6
d) 8

(36) Which one is the Universal Gate?
a) AND
b) NAND

c) XOR d) OR

(37) An address of main memory is

a) Logical Address b) Physical Address

c) Virtual Address d) None of these

(38) The average time required to reach a storage location in memory and obtain its content s is called the

a) seek tme b) turnaround time

c) access time d) transfer time

(39) A major advantage of direct mapping of a cache is its simplicity. The main disadvantag e of this organization that

a) it does not allow simultaneous access to the i ntended data and its tag b) it is more expensive than other types of c ache organizations

c) the cache hit ratio is degraded if two or more blocks used alternately map onto the same bl ock frame in the cache d) its access time is greater than that of other ca che organizations.

(40) In which cache mapping process, memory is divided into index and tag field?

a) Associative Mapping b) Set-Associative Mapping

c) Direct Mapping d) None of these

(41) User view of memory is possible in which memory management scheme?

a) Paging b) Segmentation

c) Segmentation with paging d) None of these

(42) The Cache memory works on the principle of

a) Locality of data b) Locality of instruction

c) Locality of reference d) Locality of availability

(43) Which of the following method suffers from internal fragmentation?

a) Paging b) Segmentation

c) Segmentation with paging d) None of these

(44) If the main memory is of 8K bytes and the cache memory is of 2K words. It uses associ ative mapping. Then each word of cache memory shall be

a) 11 bit b) 21 bit

c) 16 bit d) 20 bit

(45) What is the content of Stack Pointer (SP)?

a) Address of the current instruction b) Address of the next instruction

c) Size of the stack d) Address of the top element of the stack

(46) The cache memory of 1K words uses direct mapping with a block size of 4 words. Ho w many blocks can the cache accommodate?

a) 256 Word b) 512 Word

c) 1024 Word d) 128 Word

(47) If a system is 64 bit machine, then the length of each word will be

a) 4 bytes b) 8 bytes

c) 16 bytes d) 12 bytes

(48) Which one is used to implement virtual memory organization?

a) Page table b) Frame table

c) MMU d) None of these

(49) Which of the following is lowest in memory hierarchy?

a) Cache memory
b) Secondary memory
c) RAM
d) Register

(50) If memory access takes 20 ns with cache and 110 ns without it, then the Hit ratio (cach e uses a 10 ns memory) is

a) 87%
b) 88%
c) 90%
d) 93%

(51) A page fault

a) Occurs when there is an error in a specific pa ge
b) Occurs when a program accesses a page o f main memory
c) Occurs when a program accesses a page not currently in main memory
d) Occurs when a program accesses a page b elonging to another program

(52) Access time is small for

a) ROM
b) SRAM
c) DRAM
d) Register

(53) Which memory is non volatile and may be written only once?

a) RAM
b) EEROM
c) EPROM
d) PROM

(54) Which of the following registers is used to keep track of address of the memory locatio n where the next instruction is located?

a) Memory Address Register
b) Memory Data Register
c) Instruction Register
d) Program Counter

(55) The register used as a working area in CPU is

a) PC
b) IR
c) MAR
d) Accumulator

(56) Which among the following is not a method of accessing data?

a) Sequential
b) Asynchronous
c) Random
d) None of these

(57) How long does a static SRAM holds data?

a) Eternally
b) Until power is supplied
c) Only during manufacturing
d) None of these

(58) Which of the following is not a performance metrics of linear pipeline processor?

a) Speed-Up
b) Efficiency
c) Throughput
d) None of the above

(59) Data flow through the pipeline processor is represented by

a) Space-Time diagram
b) Gnat chart
c) Pie chart
d) Graph

(60) Time – space span are of _____ types

a) 1
b) 2
c) 3
d) 4

(61) Which connection is present in omega network?

a) Shuffle
b) Exchange
c) Cube
d) Butterfly

(62) In multistage butterfly network, last connection will be

a) Butterfly connection
b) Shuffle connection

c) Exchange connection
d) Inverse-shuffle connection

(63) The processing elements present in Flynn's classification is actually

a) CPU
b) ALU
c) CU
d) None of these

(64) Which one does not exist in real life?

a) SISD
b) SIMD
c) MISD
d) MIMD

(65) Which one is better?

a) Pipelined processor
b) VLIW processor
c) Super-pipelined processor
d) Both (b) and (c)

(66) Which one is not a performance metrics of pipeline processor?

a) Speed-up
b) Efficiency
c) Throughput
d) All of these

(67) Which one is also called as Omega network?

a) Single stage Shuffle-Exchange interconnection network
b) Multi stage Shuffle-Exchange interconnection network
c) Single stage cube interconnection network
d) Multi stage cube interconnection network

(68) In mesh connected ILLIAC network, number of PE are

a) 4
b) 16
c) 32
d) 64

(69) Which of the following gives CPI<1

a) Pipelining
b) Super-pipelining
c) Super-scalar
d) Both (b) and (c)

(70) Which of the pipeline hazard caused by the branch instructions?

a) Control Hazard
b) Structural Hazard
c) Data Hazard
d) All of these