BRAINWARE UNIVERSITY

Term End Examination 2023
Programme – B.Tech.(CSE)-2018/B.Tech.(CSE)-2019
Course Name – Advanced Computer Architecture
Course Code - PEC-702B
(Semester VII)

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Brainware University
Barasat, Kolkata -700125

Full Marks : 70 **Time : 3:0 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Express which one is the representation of data flow in general pipeline processor?
a) Space-Time diagram b) Gantt Chart
c) Reservation Table d) Pie Chart

(ii) Identify in which processor, loop control overhead is minimized?
a) Scaler Processor b) Vector Processor
c) IAS Processor d) Multiprocessor

(iii) write the snoopy Protocol is the solution of
a) Vector Fitting b) Pipeline Hazard
c) Cache Coherence d) Bus Contention

(iv) Select which bus is bidirectional?
a) Address b) Data
c) Control d) All of these

(v) Explain which of the following gives CPI<1?
a) Array processor b) VLIW
c) Scalar Processor d) None of these

(vi) Define in which of the following is the first field in vector instruction format?
a) Base Address b) Address Offset
c) Operation Code d) Length

(vii) State that the scaler-Vector Product is a _____ operation.
a) Unary b) Binary
c) Ternary d) All of the above types

(viii) Identify that the starting address is also known as
a) Address offset b) Base address
c) Displacement d) None of the above

(ix) Choose which of the following is not a data hazard?
a) RAR b) RAW
c) WAR d) WAW

(x) Choose in which of the following processor is a vector processor?

a) BSP
b) ILLIAC-IV
c) PEPE
d) TI-ASC

(xi) Choose that the vector Stride value is used to access_____ vectors.

a) One dimensional
b) Two dimensional
c) Three dimensional
d) Multidimensional

(xii) If a vector has 10 X 10 = 100 elements in row-major fashion, then calculate to access the elements according to column will be

a) 1
b) 2
c) 5
d) 10

(xiii) Express that the addition is the responsibility of

a) ALU
b) CU
c) Register Set
d) None of the above

(xiv) Express which one has select lines?

a) Encoder
b) Decoder
c) Multiplexer
d) De-multiplexer

(xv) Choose which one is not a data hazard?

a) RAR
b) RAW
c) WAR
d) WAW

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Group-B

(Short Answer Type Questions) 3 x 5=15

2. Compare between RISC and CISC. (3)
3. Write a short note on Instruction Cycle. (3)
4. Write a short notes on multiprocessor. (3)
5. Explain what are the vector length and stride issues in a vector processor? (3)
6. Explain what is cache coherence problem and the solution of it? (3)

OR

What are the different performance metrics of a computer memory? Explain with example. (3)

Group-C

(Long Answer Type Questions) 5 x 8=40

7. Evaluate a multistage Shuffle-Exchange interconnection network for N=16 with diagram (5)
8. Draw the block diagram of a vector processor and explain each of the part. (5)
9. Describe the register-to-register and memory-to-memory architecture? (5)
10. Explain the following: The size of cache memory and the speed of a system is proportional. (5)
11. Explain the following: The size of cache memory and the speed of a system is proportional. (5)
12. What is Space-Time Diagram? Explain with an example of five process pipeline. (5)
13. What is virtual memory? Explain the functionality of it with a real life example. (5)
14. Draw both single-stage and multistage cube interconnection network & justify it. (5)

OR

Explain what is Logical and physical address space? How they are related to MMU? (5)

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