



## **BRAINWARE UNIVERSITY**

## Term End Examination 2023 Programme – MCA-2020/MCA-2021/MCA-2022 Course Name – Computer Architecture and Microprocessor Course Code - MCA103 ( Semester I )

Full Marks : 60 Time : 2:30 Hours

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

## Group-A

(Multiple Choice Type Question)

1 x 15=15

- 1. Choose the correct alternative from the following:
- (i) Infer stack
  - a) 32-bit register in the microprocessor
  - c)
    - 16-bit register in the microprocessor
- b) 16-bit memory address stored in the h program counter
- d) Set of memory locations in R/W memory reserved for storing information temporarily during the execution of a program
- (ii) Corelate one field where operation is normally specified in
  - a) Opcode

b) Operand

c) Instruction

- d) Operation
- (iii) Judge the computer architecture aimed at reducing the time of execution of instructions
  - a) CISC

b) RISC

c) ISA

- d) None of these
- (iv) Choose the iconic feature of the RISC machine
  - a) Increased memory size

b) Reduced number of addressing modes

c) Larger memory space

- d) Having a branch delay slot
- (v) Anticipate the binary address issued to data or instructions
  - a) Physical address

b) Location

c) Relocatable address

d) Logical address

- (vi) Anticipate full form of VLSI
  - a) Very Large-Scale Integration
  - c) Volatile Layer System Interface

- b) Very Large Stand-alone Integrationd) Volatile Large System Interface
- (vii) Select alternate name of Boolean Algebra.
- a) Transistor algebra

b) Gate algebra

		n contacting algebra	
	c) Counting algebra	d) Switching algebra	
(viii)	Recall the gate which is used to find sum circuit		
	a) XOR	b) XNOR	
	c) AND	d) OR	
(ix)	x) State the number of bits required to store one BCD digit.		
	a) 1	b) 2	
	c) 3	d) 4	
(x)	JK flip-flop converts to if J=K.	,	
	a) Shorted JK flip-flop	b) SR flip-flop	
	c) T flip-flop	d) K flip-flop	
(xi)	For a decoder circuit with 4 input lines, identify	what will be the output for bitwise	
(***)	input of 0111		
		b) 000000010000000	
	a) 00000000000111	d) 00000001111111	
/s.::\	c) 00000001000000	a) 00000001111111	
(XII)	(xii) Predict the binary equivalent of -1		
	a) 111	b) 1111	
	c) 11	d) None of these	
(xiii) Determine which register can interact with the secondary storage			
	a) PC	b) SP	
	c) MAR	d) MBR	
(xiv	Predict the addressing mode used in instruction	n ADD X, Y	
	a) Absolute	b) Immediate	
	c) Relative	d) Indirect	
(yy			
(xv) Discover the number of instructions needed to add 'n' numbers and store the result in memory using only one address instructions			
	a) n	b) n - 1	
	c) n + 1	d) Independent of n	
Group-B			
(Short Answer Type Questions) 3			3 x 5=15
2. Compute Gray code with a suitable example.			(3)
3. Illustrate RISC.			(3)
4. Calculate (78.56) decimal into Hexadecimal equivalent.			(3)
5. Develop Magnitude comparator.			(3)
6. Differentiate between DRAMs and SRAMs			(3)
	OR		
Discuss maskable and non-maskable interrupts.			(3)
Group-C			
	(Long Answer	Type Questions)	5 x 6=30
		,	
7	Compare SRAM and DRAM.		/m\
8.	•	ale precision format	(5)
<ul><li>8. Compute decimal value 123.25 in IEEE 754 single precision format.</li><li>9. Discriminate Hardware and Software Interrupts.</li></ul>			(5)
10. Analyse Cache Memory.			(5)
			(5)
11. Construct a Memory of capacity 1024 X 8 using 512 X 8 RAM and 512 X 8 ROM.			(5)
12. Name are the interrupt pins of the 8085 microprocessor including maskable and non-maskable interrupts.			(5)
	OR		
State Intel 8085A architecture			
	State litter 6063A dictillecture.		(5)

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