BRAINWARE UNIVERSITY

Term End Examination 2023
Programme – B.Tech.(ECE)-2019
Course Name – Digital System Design
Course Code - PCC-EC302
(Semester III)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Select the two inputs of the NAND gate if the output is low

a) 0 b) 1
c) 10 d) 11

(ii) Find the value of X if (734)8 = (X)16

a) C 1 D b) D C 1
c) 1 C D d) 1 D C

(iii) Identify the code where all successive numbers differ from their preceding number by single bit -

a) Binary code b) BCD
c) Excess – 3 d) Gray

(iv) When an input signal A=11001 is applied to a NOT gate serially, its output signal is represented as

a) 111 b) 110
c) 10101 d) 11001

(v) The fastest logic in logic families is indicated as

a) ECL b) TTL
c) CMOS d) LSI

(vi) Convert (0.345)10 into an octal number

a) (0.16050)8 b) (0.26050)8
c) (0.19450)8 d) (0.24040)8

(vii) According to the property of minterm, calculate how many combination will have value equal to 1 for K input variables?

a) 0 b) 1
c) 2 d) 3

(viii) How many Flip-Flops are required to construct mod–16 counter?

a) 5 b) 6
c) 3 d) 4

(ix) Choose the output for a 1:4 demultiplexer, if the two control inputs are C1 = 1 & C2 = 1

a) Y0 b) Y1
c) Y2 d) Y3

(x) Calculate how many two input AND gates and two input OR gates are required to realize Y = BD+CE+AB

a) 1, 1 b) 4, 2
c) 3, 2 d) 2, 3

(xi) Calculate minimum number of two input NAND gates required to realize XOR gate

a) 3 b) 4
c) 5 d) 6

(xii) Which of the following circuits consider under the class of sequential logic circuits?
1.Full adder 2. Full subtractor 3. Half adder 4. J-K flip 5. Counter

a) 1 and 2 b) 2 and 3
c) 3 and 4 d) 4 and 5

(xiii) Choose a logic circuit that accepts several data inputs and allows only one of them at a time to get through to the output

a) multiplexer b) demultiplexer
c) transmitter d) receiver

(xiv) How many NOT gates are required for the construction of a 4-to-1 multiplexer?

a) 3 b) 4
c) 2 d) 5

(xv) To design a sequential circuits. the present input depends on

a) past inputs only b) present inputs only
c) present as well as past inputs d) past outputs

Group-B
(Short Answer Type Questions) 3 x 5=15

2. Construct a full subtractor circuit using NAND gates only. (3)
3. Simplify the following expression using K-map method: Y (A, B, C, D) = Σ m (1, 3, 4, 6, 9, 11, 12, 14) (3)
4. Illustrate 1'S complement and 2'S complement with an example. (3)
5. Design a JK Flip Flop using a D Flip Flop (3)
6. Construct a full adder circuit using a 3 to 8 line decoder. (3)

OR

Construct 1 to 4 De-multiplexer using basic gates. (3)

Group-C
(Long Answer Type Questions) 5 x 6=30

7. Describe the basic features of i) DTL ii) TTL iii) ECL iv) MOS logic v) CMOS logic (5)
8. Illustrate NAND gate and demonstrate the action of NOR gate as Universal gate. (5)
9. Construct and explain the full adder circuit using two half adder circuit through a block diagram. (5)
10. Simplify the following expression using K-map and realize the simplified function using logic gates: F(A,B,C,D)=ΠM(1,2,3,7,8,9,10,11,14) (5)
11. Explain the design of a MOD 14 asynchronous UP/DOWN counter with JK flip flop. (5)
12. Distinguish between Synchronous and Asynchronous counters. (5)

OR

Discriminates between combinational circuit and sequential circuit. (5)

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