BRAINWARE UNIVERSITY

Term End Examination 2023-2024
Programme – B.Sc.(ANCS)-Hons-2021
Course Name – Computer Organization and Architecture
Course Code - BNCSC303
(Semester III)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A
(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Identify computer architecture.
- a) set of categories and methods that specify the functioning, organisation, and implementation of computer systems
- b) set of principles and methods that specify the functioning, organisation, and implementation of computer systems
- c) set of functions and methods that specify the functioning, organisation, and implementation of computer systems
- d) None of the mentioned

(ii) Memorize computer organization.
- a) structure and behaviour of a computer system as observed by the user
- b) structure of a computer system as observed by the developer
- c) structure and behaviour of a computer system as observed by the developer
- d) All of the mentioned

(iii) Locate the subcategories of computer architecture.
- a) Microarchitecture
- b) Instruction set architecture
- c) Systems design
- d) All of the mentioned

(iv) Identify the advantage of I/O mapped devices to memory mapped is _____.
- a) The former offers faster transfer of data
- b) The devices connected using I/O mapping have a bigger buffer space
- c) The devices have to deal with fewer address lines
- d) No advantage as such

(v) State that in memory-mapped I/O _____.
- a) The I/O devices and the memory share the same address space
- b) The I/O devices have a separate address space
- c) The memory and I/O devices have an associated address space
- d) A part of the memory is specifically set aside for the I/O operation

(vi) _____ are the different types of generating control signals.
- a) Hardwired
- b) Micro-instruction

c) Micro-programmed
d) Both Micro-programmed and Hardwired

(vii) Observe how the fetch and execution cycles are interleaved with the help of _____.

a) Modification in processor architecture
b) Clock
c) Special unit
d) Control unit

(viii) Identify that UNIVAC belongs to_____generations of computer.

a) First
b) Second
c) Third
d) Fourth

(ix) Define that the pipeline increases... of the processor.

a) Throughput
b) Storage
c) Predictivity
d) Latency

(x) Predict the bit used to indicate whether the block was recently used or not_____.

a) Reference bit
b) Dirty bit
c) Control bit
d) Idol bit

(xi) Identify which among the following is used by Instruction scheduling can be used to eliminate data and control hazard.

a) Schedule the execution of the instruction only if there is no hazard.
b) Using a special hardware to check for hazard and issue instructions only when possible.
c) Allowing the compiler the move instructions around to fill the LOAD/BRANCH delay slot(s) with meaningful instructions.
d) None of the above.

(xii) Indicate that the system is notified of a read or write operation by _____.

a) Appending an extra bit of the address
b) Enabling the read or write bits of the devices
c) Raising an appropriate interrupt signal
d) Sending a special signal along the BUS

(xiii) Choose the following circuit to convert the binary data into a decimal.

a) Decoder
b) Encoder
c) Code converter
d) Multiplexer

(xiv) Construct the following memory unit that communicates directly with the CPU.

a) Auxiliary memory
b) Main memory
c) Secondary memory
d) None of the above

(xv) A collection of 8 bits is called a ____. Identify.

a) Byte
b) Nibble
c) Word
d) Record

Group-B

(Short Answer Type Questions) 3 x 5=15

2. Define a mainframe computer. (3)
3. Discover the fundamental difference between Von Neumann and Harvard architectures. (3)
4. Define a device driver, and why is it essential for CPU-device communication. (3)
5. Discover pipelining in computer organization. (3)
6. What is EEPROM, and analyse how is it different from traditional ROM? (3)

OR

What is paging, and analyse how does it work? (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Explain two address instruction format with example. (5)
8. Explain Memory hierarchy. (5)

9. Define RAM and its variations. (5)
10. Analyse the advantages of pipe lining. (5)
11. Explain Three address instruction format with example. (5)
12. Analyse the different phases of Instruction Cycle. (5)

OR

Analyse at least 5 different addressing modes. (5)

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