



## **BRAINWARE UNIVERSITY**

Term End Examination 2023-2024 Programme - Dip.CSE-2022 Course Name - Digital Electronics Course Code - DCSE-PC302 ( Semester III )

Full Marks: 60

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question)

1 x 15=15

Time: 2:30 Hours

- Choose the correct alternative from the following:
- (i) Identify the Universal Gate
  - a) AND

b) OR

c) NAND

- d) XOR
- (ii) Memorize that each decimal digit is represented by \_\_\_\_ bits binary number
  - a) 1 c) 3

b) 2 d) 4

- (iii) Identify the Derived Gate
  - a) AND

- b) OR d) XOR
- c) NAND (iv) Select the correct base of Octal number system
  - a) 2

b) 8

c) 10

- d) 16
- (v) In K-Map, individual cells are observed as
  - a) Binary code

b) Grey Code

c) BCD Code

- d) None of these
- (vi) Discover the primary purpose of the JK flip-flop\'s J and K inputs
  - a) Toggling the output

b) Setting the output

c) Clearing the output

- d) Inverting the output
- (vii) Select the correct option for full adder
  - a) 1 imput and one output

b) 2 input and one output

c) 3 input and 2 outputs

- d) 2 inputs and three outputs
- (viii) What happens when the clock input of an SR flip-flop is high and the S and R inputs are both low? Choose the correct option
  - a) The Q output is set to 1

- b) The Q output is set to 0
- c) The flip-flop enters an undefined state
- d) The flip-flop toggles
- (ix) What are the two types of basic adder circuits? Select the correct alternative

		a) Sum and carry	d) One and two's-complement	
	(x)	c) Asynchronous and synchronous Choose: Which flip-flop type is known for its ale edge when both J and K inputs are high?	oility to toggle its output on each o	lock
	(xi)	a) JK flip-flop c) D flip-flop BCD adder can be constructed with 3 IC package	b) T flip-flop d) SR flip-flop ges each of Select the	correct
		alternative		
		a) 2-bits	b) 3-bits d) 5-bits	
0	Riv	c) 4-bits  Discover the primary role of a Master/Slave flir	a) 5-bits	
0	· (All)	a) Storing hinary data	b) Counting clock pulses	
,	c) 4-bits d) 5-bits d) 5-bits d) 5-bits d) 5-bits d) 5-bits d) 5-bits d) 6-bits d) 6-bits d) 6-bits d) 6-bits d) 7-bits d) 8-bits d) 8-bits d) 6-bits d) 6-bits d) 7-bits d) 8-bits d) 8-b		<ul> <li>d) Multiplexing inputs</li> <li>ed for selecting a single input fror</li> </ul>	n
	(Alli)	multiple inputs & directing the binary informat	tion to output line?	
		a) Data Selector	b) Data distributor	
		c) Both data selector and data distributor	d) DeMultiplexer	correct
	(xiv)	What is the primary function of a clock signal in option	n a sequential circuit? Choose the	Correct
		a) Synchronizing the operations	b) Controlling the power suppl	y
		c) Clearing the flip-flops	d) Generating random number	lect
	(xv)	If the number of n selected input lines is equal lines. Estimate and select the correct alternative	to 2°m then it requiresse	
		a) 2	b) m	
		n) 2	d) 2n	
			up-B	3 x 5=15
		(Short Answer	Type Questions)	2 X 2=12
	2 Def	ine the decimal number system.		(3)
<ul><li>3. Describe the key difference between a Half Adder and a Full Adder.</li><li>4. Explain why Input clock of RS flip-flop is given to Pulser</li><li>5. Describe universal shift register.</li></ul>				(3)
				(3)
				(3)
6. Analyze the key characteristics of a double-digit counter.			(3)	
			OR .	(3)
	Expl	ain the principle behind a synchronous count	er.	(3)
		Gro	up-C	
			ype Questions)	5 x 6=3
7.	des	lain the operation of a Master/Slave Flip-Flo ign. Apply this knowledge to design a Maste ction and write down the truth table.	p and its advantages in sequent r/Slave JK flip-flop circuit for a to	ial circuit (5) oggle
0	Fund	ain the significance of reprogrammability in	memory devices, focusing on E	EPROM and (5)
٥.	EPR	OM, and evaluate the implications of their r	eprogrammable nature for system	em flexibility
0	and	reliability. uate the role of memory hierarchy in moder	rn computer architectures, cons	sidering the (5)
9.	use	of both RAM and ROM components. Explain	how this hierarchy optimizes of	data storage
		access in computer systems.		(5)
10.	Expl	ain Full Subtractor with proper diagram		(3)

- 11. Describe minimize the boolean expression Y = ABC'D + ABC'D' + ABCD + ABC'D' + ABCD' + ABC'D' + A(5)
- 12. Assess the economic and environmental implications of using EPROM and EEPROM in consumer electronics and assess the reasons behind the shift towards more (5) environmentally friendly memory solutions.

Evaluate the role of RAM in improving the overall performance of a computer system. Assess the impact of factors like cache memory size, data bus width, and memory access speed on system efficiency.

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(5)