BRAINWARE UNIVERSITY

Term End Examination 2023-2024
Programme – Dip.EE-2021
Course Name – Basic Electronics
Course Code - DEE303
(Semester III)

Time : 2:30 Hours

Full Marks : 60

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Choose the base current amplification factor β is given by
a) IC/IB b) IB/IC
c) IE/IB d) IB/IE

(ii) Tell, the doping of the emitter region of a transistor is
a) Larger than that of collector region b) Less than that of collector region
c) Equal to that of collector region d) None of these

(iii) Select the option for which semiconductor diode is used
a) oscillator b) rectifier
c) amplifier d) None of these

(iv) Cite the acceptor impurities
a) Generate electrons b) Generate holes
c) Generate hole and electrons d) All of these

(v) If FET employed in cut-off, the depletion layers are
a) Touching each other b) Close together
c) Far apart d) None of these

(vi) A FET produce output due to
a) Majority carriers only b) Minority carriers
c) Positive and negative ions d) Positively charged ions

(vii) Identify the option which represent p-n junction diode's dynamic conductance is directly proportional to
a) The applied voltage b) The temperature
c) Its current d) None of these

(viii) During reverse bias, a small current develops which is named as
a) Forward current b) Reverse current
c) Reverse saturation current d) Active current

(ix) Identify which of the following is true in construction of a transistor?

a) The collector dissipates less power
b) The emitter supplies minority carriers
c) The collector is made physically larger than the emitter region
d) The collector collects minority charge carriers

(x) Identify the Universal Gate

a) AND
b) OR
c) NAND
d) XOR

(xi) Identify the terminal of JFET

a) anode, cathode, grid
b) emitter, base, collector
c) source, gate, drain
d) none of them

(xii) Choose cut off voltage if the pinch off voltage of JFET is 5V.

a) 2.5 V
b) 5 V
c) 7.5 V
d) 0 V

(xiii) Relate between alpha and beta

a) beta = 1+(alpha-1)
b) alpha = beta / (beta + 1)
c) alpha= beta /(beta - 1)
d) beta = 1/(1 - alpha)

(xiv) Identify active region of a transistor

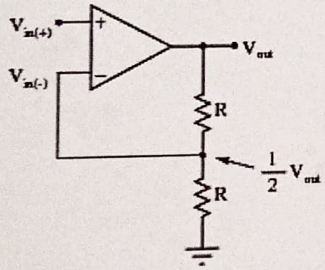
a) Both emitter and collector junctions are reverse biased
b) Both emitter and collector junctions are reverse biased
c) Emitter junction is forward biased and collector junction is reverse biased
d) None of these

(xv) For a p-n-p transistor in CE mode, β=100, then identify the value of α of the transistor

a) 0.99
b) 0.099
c) 9.9
d) 99

Group-B

(Short Answer Type Questions) 3 x 5=15

2. Explain feedback and why it is required. (3)
3. Develop the gain of a system with negative feedback. (3)
4. Explain different series feedback amplifier topologies. (3)
5. Explain different shunt feedback amplifier topologies. (3)
6. 

Write the transfer function (input/output equation) for an operational amplifier with an open-loop voltage gain of 100,000, and the inverting input connected to a voltage divider on its output terminal (so the inverting input receives exactly one-half the output voltage). In other words, develop an equation describing the output voltage of this op-amp (Vout) for any given input voltage at the non-inverting input (Vin():

OR (3)

$$V_o = \frac{R_3}{R_1 + R_3} \frac{R_2 + R_4}{R_2} V_1 - \frac{R_4}{R_2} V_2$$

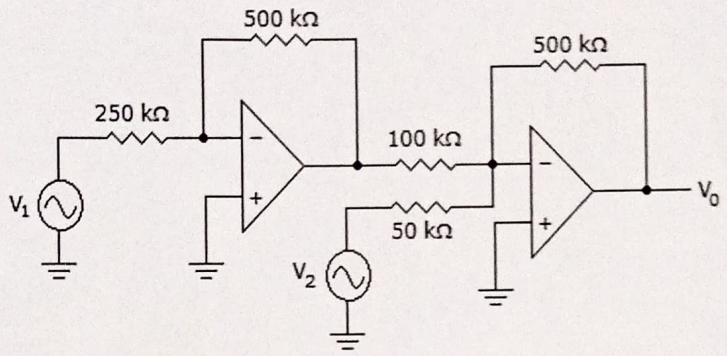
Propose how many op-amps are required to implement this equation?

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Explain the functionality of 3:8 decoder (5)
8. A JFET has I_{DSS}= 12 mA and $V_{GS(off)}$= -4V. Determine the minimum value of V_{DD} required to put the device in the constant current region of operation. (5)

9. (5)



Evaluate the output voltage V_o if $V_1 = -V_2 = 300$ mV.

10. Describe the various methods used for transistor biasing. (5)
11. Explain base resistor method of transistor biasing. (5)
12. Design an non - inverting amplifier and derive its gain. (5)

OR

Design a subtractor circuit using op-amp. (5)

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