BRAINWARE UNIVERSITY

Term End Examination 2023-2024
Programme – Diploma in Robotics & Automation-2022
Course Name – Digital Electronics
Course Code - ECPC303
(Semester III)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) The gates required to develop a half adder are

a) EX-OR gate and NOR gate
b) EX-OR gate and OR gate
c) EX-ORgate and AND gate
d) Four NAND gates.

(ii) Karnaugh map is chosen for the purpose of

a) Reducing the electronic circuits used
b) To map the given Boolean logic function
c) To minimize the terms in a Boolean expression
d) To maximize the terms of a given a Boolean expression

(iii) In a 3-variable Karnaugh Map, determine how many cells are there?

a) 4
b) 8
c) 16
d) 32

(iv) Identify which input values will cause an AND logic gate to produce a HIGH output?

a) At least one input is HIGH
b) At least one input is LOW
c) All inputs are HIGH
d) All inputs are LOW

(v) Identify what is the octal equivalent of the binary number: 10111101

a) 675
b) 275
c) 572
d) 573

(vi) To create a combinational circuit, the output depends on the

a) Input combination at the time
b) Input combination and the previous output
c) Input combination at that time and the previous input combination
d) Present output and the previous output

(vii) If A, B and C are the inputs of a full adder then the carry is produced by

a) A AND B OR (A OR B) AND C
b) A OR B OR (A AND B) C
c) (A AND B) OR (A AND B)C
d) A XOR B XOR (A XOR B) AND C

(viii) Choose the desired logic circuits which accept two binary digital on inputs and produces two binary digital, a sum bit and carry bit on its outputs?

a) full adder
b) half-adder

c) serial adder
d) parallel adder

(ix) Determine the number of select lines to construct a 8 – to – 1 multiplexer

a) 2
b) 3
c) 4
d) 5

(x) The binary representation of BCD number 00101001 is recognized as

a) 11101
b) 110101
c) 1101001
d) 101011

(xi) When an input signal A=11001 is applied to a NOT gate serially, its output signal is identified as

a) 111
b) 110
c) 10101
d) 11001

(xii) Select the decimal equivalent of Binary number 10101

a) 21
b) 31
c) 26
d) 28

(xiii) Identify the digital logic family which has the lowest propagation delay time is

a) ECL
b) TTL
c) CMOS
d) PMOS

(xiv) Identify the binary equivalent of hexadecimal number FA

a) 1010 1111
b) 1111 1010
c) 10110011
d) none of these

(xv) Determine the number of cells in a 6-variable K-map

a) 6
b) 12
c) 36
d) 64

Group-B

(Short Answer Type Questions) 3 x 5=15

2. Construct Ex-NOR gate using NAND gates only (3)

3. Describe NAND gate with its Boolean expression, truth table and logical symbol. Show how it can be realized by using basic gates. (3)

4. Apply Boolean algebra to simplify the expression (3)

$$Y = (\overline{A} + B) \cdot (A + B)$$

5. Apply K-map to simplify the following expression Y (A, B, C, D) = Σ m (1, 3, 4, 6, 9, 11, 12, 14) (3)

6. Explain D flip-flop with present state-next state table and excitation table (3)

OR

Discriminates between combinational circuit and sequential circuit. (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Design a full adder circuit using a 3 to 8 line decoder. (5)

8. Apply K-map to simplify the following expressions (5)
   (a) $F(A,B,C,D) = \Sigma m (1,3,7,11,15) + \Sigma d (0,2,5)$
   (b) $F(A,B,C,D) = \Sigma m (0,2,3,6,7) + \Sigma d (8,10,11,15)$

9. Explain J-K flip-flop with present state-next state table, excitation table and logical expression of next state output (5)

10. Describe NAND gate and demonstrate the action of NAND gate as Universal gate. (5)

11. Describe: i) Noise margin ii) Fan-out iii) Fan-in iv) Propagation delay v) Power dissipation (5)

12. Construct 4:1 Multiplexer using three 2:1 Multiplexer. (5)

OR

Construct 16:1 multiplexer using 4:1 multiplexer only. (5)

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