BRAINWARE UNIVERSITY

Term End Examination 2023
Programme – Dip.EE-2019/Dip.EE-2021
Course Name – Applied and Digital Electronics
Course Code - DEE404
(Semester IV)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A
(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Any signed negative binary number is identified by its _____
a) MSB b) LSB
c) Byte d) Nibble

(ii) The parameter through which 16 distinct values can be represented is known as _____
a) Bit b) Byte
c) Word d) Nibble

(iii) According to the property of minterm, calculate how many combination will have value equal to 1 for K input variables?
a) 0 b) 1
c) 2 d) 3

(iv) A variable on its own or in its complemented form is written as a _____
a) Product Term b) Literal
c) Sum Term d) Word

(v) On multiplication of (10.10) and (01.01), we produced _____
a) 101.001 b) 10.101
c) 11.001 d) 110.0011

(vi) Maxterm is the sum of _____ of the corresponding Minterm with its literal complemented.
a) Terms b) Words
c) Numbers d) Nibble

(vii) 1's complement of 1011101 is _____
a) 101110 b) 1001101
c) 100010 d) 1100101

(viii) There are _____ Minterms for 3 variables (a, b, c).
a) 0 b) 2
c) 8 d) 1

(ix) All input of NOR as low produces result as _____

a) Low b) Mid
c) High d) Floating

(x) RTL constructs of a common emitter stage with a _____ connected between the base and the input voltage source.

a) collector b) base resistor
c) capacitor d) inductor

(xi) Select the input given to "R" when SR flip – flop is converted to JK flip – flop?

a) K.Q b) K.Q'
c) J.Q d) J.Q'

(xii) Which of the following options represent the correct reduction of XYZ + XYZ ?

a) 0 b) YZ
c) X + X d) 2YZ

(xiii) Select which of these pins will allow to activate and deactivate a multiplexer?

a) Enable pin b) Selection pin
c) Logic pin d) Preset pin

(xiv) Calculate how many entries will be in the truth table of a 4-input NAND gate?

a) 6 b) 8
c) 32 d) 16

(xv) Show the Division of the binary number: 111001 ÷ 1101 and find the reminder

a) 1010 b) 110
c) 101 d) 11

Group-B

(Short Answer Type Questions) 3 x 5=15

2. What is priority encoder? Give a brief demonstration on Encoder. (3)
3. What is Master slave J-K flip flop? Explain race around condition (3)
4. Demonstration on D Flip Flop. (3)
5. Explain fan in and fan out. (3)
6. Analyze the two hazards that can be there in a combinational circuit? (3)

OR

Explain how to avoid static hazards in a combinational circuit(single variable change hazards)? (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. i) Illustrate NAND gate. ii) Establish the action of NAND gate as Universal gate. (5)
8. Represent a full-subtractor using fewer (i) NAND gates, (ii) NOR gates. (5)
9. Explain the design of a MOD 14 asynchronous UP/DOWN counter with JK flip flop. (5)
10. Illustrate NOR gate and demonstrate the action of NOR gate as Universal gate. (5)
11. Compare the performance of binary serial and parallel adders. (5)
12. Design a SR Flip Flop using JK Flip Flop with suitable explanation. (5)

OR

(a) Write down the applications of four basic flip flop? (b) Show how RS flip-flop can be obtained by using gates only. Describe its action. Give its symbol and truth table (5)

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