



BRAINWARE UNIVERSITY

Term End Examination 2023

LIBRARY Brainware University Barasat, Kolkata -760125

STORT MENTAN MERSEN

Programme - Dip.EE-2019/Dip.EE-2021

Course Name - Applied and Digital Electronics

Course Code - DEE404 (Semester IV)

Full Marks: 60

c) 4

Time: 2:30 Hours

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

5=15

		Group-A	
	(Multiple Choice Type Question)		1 x 1
1.	Choose the correct alternative from the fol	lowing :	
(i)	If the decimal number is a fraction then it the number continuously by 2.	s binary conversion is obtained by	•
	a) Dividing c) Adding	b) Multiplyingd) Subtracting	
	2's complement of 11001011 is written a) 1010111 c) 110101 Binary coded decimal is a collection of	b) 11010100 d) 11100010	
	a) Two binary digits c) Four binary digits The decimal number 10 is represented in	b) Three binary digitsd) Five binary digits	
	a) 10100000 c) 10000 In Digital Circuits, identify which of the fol control inputs in a T flip flop?	b) 1010111 d) 101011 lowing options represent the synchronous	
(vi)	a) Tc) ClockCalculate the distance is required for an e analysis?	b) 0 d) 1 rror correction according to Hamming's	
(vii)	a) 1 c) 3 Write how many cycles of addition and sh perform multiplication using the shift met	b) 2 d) 4 ifting in a 4 – bit multiplier are required to :hod?	
	a) 1	b) 2 d) 8	

connecting 4 flip – flops in cascade?	sed clock signal can be obtained by			
a) 2	b) 4			
c) 8	d) 16			
(ix) Show the addition of the binary number 10	Show the addition of the binary number 101001+ 010011			
a) 10100	b) 111100			
c) 111	d) 101110			
(x) A digital circuit that can store only one bit is	s a representation of			
c) Flip flop	b) NOR gate			
c) Flip flop	d) XOR gate			
(xi) The logical sum of two or more than two lo	gical products is produced as			
a) OR operation	b) POS			
c) SOP	d) NAND operation			
(xii) Calculate the Minterms for four variables				
a) 8	b) 16			
c) 2	d) 1			
(xiii) A K-map (Karnaugh map) is an abstract form		5		
matrix				
a) Block diagram	b) Cycle diagram			
c) Square diagram	d) Venn diagram			
(xiv) Identify which of the following gates has the possible input combinations?	e exact inverse output of the OR gate for al	I		
a) AND	b) NOT			
c) NOR	d) NAND			
(xv) Full adder is used to predict				
a) 2 bit addition	b) 3 bit addition			
c) 4 bit addition	d) 6 bit addition			
G	iroup-B			
(Short Answe	er Type Questions)	3 x 5=15		
2. Demonstrate on Multiplexer		(3)		
3. What is the difference between RAM and ROM.				
4. Construct Half Subs-tractor using Gates				
5. Illustrate Maxterm and Minterm.				
6. Design a circuit for 3-input majority function using a 4:1 Mux? OR				
A full adder can be implemented using basic gain implementation among them, which needs mi		(3)		
G	roup-C			
(Long Answe	er Type Questions)	5 x 6=30		
7. Generalize the Canonical SOP Expression (i) Y		(5)		
 Compute the binary subtraction 1101-1011 b subtraction 1110-1111 by 2s complement me 	ethod.	ary (5)		
9. Explain the CMOS inverter gate with circuit di		(5) (5)		
10. Construct the following function using 8:1 multiplexer				
11. Explain the construction of S-R flip flop using D flip flop				
12. Write down the applications of multipleyer		(5)		

Design a half subtractor using basic gates.

ds 1005. Signal and si

LIBRARY
University
Brainware University
Rarasat, Kolkawa - 700125