



BRAINWARE UNIVERSITY



Term End Examination 2023 Programme – B.Tech.(CSE)-2018/B.Tech.(CSE)-2019/B.Tech.(CSE)-2020 Course Name – Computer Organization and Architecture Course Code - PCC-CS401 (Semester IV)

Full	Marks: 70		Time: 3:0 Hours	
ĮT	he figure in the margin indicates full marks. Cand own words as far	as practicable.]		
	Group			
1.	(Multiple Choice T Choose the correct alternative from the following		15	
(i)	Identify what 32-bit representation of the decin	nal number is known as		
(iii)	a) Double-precision c) Extended format Write what is the base of Hexadecimal number	b) Single-precision d) None of these		
	a) 2 c) 10 When power is switched off which memory lose	b) 8 d) 16		
	a) Non-Volatile Memory c) Both A and B Apply signed-magnitude binary division and fin and divisor is (10011)2	b) Volatile Memory d) None		
(v)	a) 10100 c) 11001 Write the number which is numerically equal to	b) 100 d) 1100 o (100110)2		
(vi	a) (46)8 c) (36)10) Auxillary memory access time is generally Identify the correct answer?	b) (2A2)H d) (26)10 times that of the main memory.		
(vii	a) 10 c) 1000 i) Identify the correct example for Auxiliary Mem	b) 100 d) 10000 nory ?		
(vii	a) Magnetic disks c) Flash memory i) Select the true statement about Adder-subtractions	b) Tapes d) Both A and B ctor composite unit		
0.700	a) It can add as well as subtract two numbers	b) At a time, it either adds or subtracts		

	c) It mainly operates with parallel adder	d) All of these		
(ix)	Select the correct answer in which all intern			
	a) CPA	b) CLA		
	c) Both	d) None of these		
(x)	Choose the next level of memory hierarchy	after the 12 cache is		
(~)				
	a) Secondary storage	b) Main memory		
	c) Register	d) TLB		
(XI)	Size of the memory mainly dependent the correct answer.	ds on the size of the address bus analyze,		
	a) Main	b) Virtual		
	c) Secondary	d) Cache		
(xii)	If M denotes the number of memory location			
-	estimate the storage capacity is	Land the state of the state of the state of		
	a) M*N	b) M+N		
	c) 2M+N	d) 2M-N		
/wiii				
(XIII) Select which of the following memory is not			
	a) RAM	b) ROM		
	c) Cache	d) ROM and Cache		
(xiv) Select which of the following is the lowest in	n the computer memory hierarchy?		
	a) Cache	b) RAM		
	c) Secondary memory	d) CPU registers		
(xv	Identify which of the following is a part of the	ne Central Processing Unit?		
(,,,,		b) Desktop		
	a) Printer	d) Mouse		
	c) ALU	4)		
	G	roup-B		
		er Type Questions)	3 x 5=15	
	(Short Allawa	. Type Queeness,		
	and the second to the second to the second to		(3)	
2. What is an Addressing Mode?				
3. E	xplain various types of Latches?	numbers using Booth algorithm.	(3) (3)	
4. C	Praw a flowchart for the multiplication of two	o processing?	(3)	
5. H	low the performance is measured in a pipelin	e processing:	(3)	
6. V	Vrite down Natural Hazards with proper expla	OP.	and a	
	Link a	OR	(3)	
٧	Vrite the memory transfer operations which a	re represented in the .	100	
		roup-C	5 x 8=40	
	(Long Answe	r Type Questions)	370 10	
			/F\	
_	Describe Von Neumann architecture with blo	ck diagram.	(5) (5)	
_	State the difference between computer organization and computer transfer			
8.	d tor ROOTH'S MUILIDIICATION discontinu			
10. I	10. Explain different types of hazards in pipelining 11. Explain three memory mapping techniques with their advantages and disadvantages			
11. E	11. Explain three memory mapping testing as			
12. E	explain direct memory access.	eline?	(5)	
13. E	xplain the problems faced in instruction pipe		(5)	
14. E	xplain cache memory	OR		
	مام عميسي	orithms with suitable example	(5)	
E	xplain Three different page replacement algo	Michigan Agent Santaria Susairi Pra		

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