BRAINWARE UNIVERSITY

Term End Examination 2023
Programme – B.Tech.(EE)]-2021
Course Name – Digital Electronics
Course Code - PCC-EE402
(Semester IV)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Logic circuits can also be constucted using _____

a) RAM b) ROM
c) PLD d) PLA

(ii) Which of the following is a type of digital logic circuit?

a) Combinational logic circuits b) Sequential logic circuits
c) Both a & b d) None of the mentioned

(iii) Which of the following options represent the synchronous control inputs in an S – R flip flop?

a) S b) R
c) Clock d) Both S and R

(iv) What must be used along with synchronous control inputs to trigger a change in the flip flop?

a) 0 b) 1
c) Clock d) Previous output

(v) What will be the output from a D flip – flop if the clock is low and D = 0?

a) 0 b) 1
c) No change d) Toggle between 0 and 1

(vi) What is the minimum distance required for single error detection according to Hamming's analysis in Digital Electronics

a) 1 b) 2
c) 3 d) 4

(vii) Identify the gate is placed between clock input and the input of AND gate to convert a positive level triggered flip – flop to a negative level triggered flip – flop?

a) NOR gate b) NOT gate
c) Buffer d) NAND gate

(viii) Recall a TTL digital circuit possess due to the presence of a multi – emitter transistor?

a) Smaller resistance b) Larger area
c) Smaller area d) Larger resistance

(ix) Select which of these flip – flops cannot be used to construct a serial shift register?

a) D – flip flop
b) SR flip – flop
c) T flip – flop
d) JK flip – flop

(x) Choose the following options is a Current – Mode logic used in Digital Circuits.

a) TTL
b) RTL
c) ECL
d) IIC

(xi) Write how many cycles of addition and shifting in a 4 – bit multiplier are required to perform multiplication using the shift method?

a) 1
b) 2
c) 4
d) 8

(xii) What kind of operation occurs in a J – K flip flop when both inputs J and K are equal to 1?

a) Preset operation
b) Reset operation
c) Clear operation
d) Toggle operation

(xiii) Select the following codes is a sequential code

a) 8421 code
b) 2421 code
c) 5421 code
d) 2441 code

(xiv) Identify what frequency division of the pulsed clock signal can be obtained by connecting 4 flip – flops in cascade?

a) 2
b) 4
c) 8
d) 16

(xv) Calculate the conversion time of a 12-bit counter type ADC with 1MHz clock frequent to convert a full scale input?

a) 4.095 μs
b) 4.095ms
c) 4.095s
d) None of the mentioned

Group-B

(Short Answer Type Questions) 3 x 5=15

2. With the help of the truth table, construct 3 to 8 line decoder using basic gates only. (3)
3. Construct Ex-OR gate using NAND gates only (3)
4. Represent XOR using minimum number of NAND gates. (3)
5. Differentiate between SRAM & DRAM. (3)
6. Describe the design of full-subtractor using two 4:1 multiplexers (3)

OR

Examine a full adder circuit using a 3 to 8 line decoder. (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Distinguish programmable ROM and non-programmable ROM (5)
8. Solve the binary subtraction 1101-1011 by 1'S complement method. ii) Make the binary subtraction 1110-1111 by 2'S complement method. (5)
9. Explain the negative edge triggered Master-slave flip flop with neat diagram (5)
10. List the five comparisons between TTL logic devices with CMOS logic devices. (5)
11. Explain the CMOS inverter gate with circuit diagram. (5)
12. Construct parallel in-parallel out, shift register (5)

OR

Create 2 input NOR gate using 1:2 DEMUX. (5)