



BRAINWARE UNIVERSITY

Term End Examination 2023-2024

Programme – B.Tech.(RA)-2021

Course Name – Nano Electronics

Course Code - PEC-ECR601B

(Semester VI)

Full Marks : 60

Time : 2:30 Hours

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question)

1 x 15=15

1. Choose the correct alternative from the following :
 - (i) Which concept describes a fundamental difference between the dynamics of the electromagnetic field (Maxwell equations) and the Schrödinger equation?
 - a) Wave nature
 - b) Momentum
 - c) Potential
 - d) Mass
 - (ii) Identify which of the following is a characteristic feature of mesostructures
 - a) They are smaller than atoms
 - b) They are larger than nanomaterials
 - c) They exist in a vacuum environment
 - d) They follow classical physics principles
 - (iii) Density of states in quantum mechanics is defined as
 - a) The probability of finding a particle at a given position
 - b) The energy levels available to a particle in a system
 - c) The rate of change of particle velocity
 - d) The distribution of particles in space
 - (iv) Select from the following which is not a characteristic of wave function
 - a) Continuous
 - b) Single valued
 - c) Differentiable
 - d) Physically Significant
 - (v) Any wave function can be written as a linear combination is described as
 - a) Eigen Vectors
 - b) Eigen Values
 - c) Eigen Functions
 - d) Operators
 - (vi) Select the component of a MOSFET which is primarily responsible for controlling the flow of current
 - a) Source
 - b) Drain
 - c) Gate
 - d) Substrate
 - (vii) For a particle inside a box, identify the length for which the potential is maximum
 - a) L
 - b) 2L
 - c) L/2
 - d) 3L
 - (viii) Determine the potential energy in those region where the wave function must not be continuous

- a) 0
c) infinite
- b) finite
d) none of these
- (ix) Indicate the primary reason for the adoption of FinFETs over traditional planar MOSFETs
- a) Higher leakage current
c) Better gate control
- b) Lower gate control
d) Lower transistor density
- (x) Identify which type of MOSFET exhibits better electrostatic control due to its 3D structure
- a) Planar MOSFET
c) Vertical MOSFET
- b) FinFET
d) None of the above
- (xi) Identify the number of concentric nano tubes for Multi walled CNT
- a) Single
c) Triple
- b) double
d) Multiple
- (xii) Indicate that the nano tube may
- a) Slides without friction.
c) Under laps without friction.
- b) Overlaps without friction.
d) Collides without friction.
- (xiii) CNT is described as a
- a) Conductor
c) Semiconductor
- b) Insulator
d) Impure metal
- (xiv) Choose which of the following effects can be caused by a rise in the temperature
- a) Increase in MOSFET current (I_{DS})
c) Decrease in MOSFET drain current (I_{DS})
- b) Decrease in BJT collector current (I_C)
d) none of these
- (xv) Choose typical value of sub-threshold slope
- a) 100 mV/decade
c) 60 mV/decade
- b) 50 mV/decade
d) 90 mV/decade

Group-B

(Short Answer Type Questions)

3 x 5=15

2. Discuss the advantage of double gate MOSFET. (3)
3. Describe IV characteristics of single electron transistor. (3)
4. Explain the properties of the wave function. (3)
5. Compare the variation of density of state for 0D, 1D, 2D and 3D system. (3)
6. Explain different types of Carbon Nanotubes based on direction of rolling. (3)

OR

Explain different types of Carbon Nanotubes based on number of sheets. (3)

Group-C

(Long Answer Type Questions)

5 x 6=30

7. State and explain different types of hybridization observed in carbon. (5)

8. Explain the criteria to achieve the Coulomb blockade. (5)

9. Differentiate Armchair carbon nanotube, Zigzag carbon nanotube, Chiral carbon nanotube. (5)

10. Justify the density of state is dependent on the dimension of a material by the following relation (5)

$$D(E) \propto E^{\frac{d}{2}-1}$$

Where d is the dimensionality of the system.

11. Discuss advantage and disadvantage of FinFET structure. (5)

12. Explain why FINFET Devices are used in place of conventional MOSFETs. (5)

OR

Explain why gate-engineering techniques are used for reduction of SCEs. (5)
