



BRAINWARE UNIVERSITY

Brainware University
Barasat, Kolkata 700125

Programme – B.Sc.(ANCS)-Hons-2019/B.Sc.(ANCS)-Hons-2020/B.Sc.(ANCS)-Hons-2019/B.Sc.(ANCS)-Hons-2020/B.Sc.(ANCS **Term End Examination 2022** 2021/B.Sc.(ANCS)-Hons-2022

Course Name – Electronics Course Code - GEEC101 (Semester I)

Full Marks: 60

Time: 2:30 Hours

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

1 x 30=30

(Multiple Choice Type Question)

1. Choose the correct alternative from the following:

(i)	Select the binary equivalent of the decimal number 368				
a)	101110000	b)	110110000		
c)	111010000	d)	111100000		
(ii)	Select the decimal equivalent of hex number	1/	A53		
a)	6793		6739		
	6973	d)	6379		
(iii)	To design a non-inverting adder inputs are applied				
a)	Non-inverting terminal	b)	Inverting terminal		
-	Both inverting and non-inverting	d)	None of these		
	terminal				
(iv)	Find the decimal equivalent number of hexadecimal number 'A0'				
a)	80	b)	256		
-	100	-,	160		
(v)	During reverse bias, a small current develops which is known as				
. , a)	Forward current	b)	Reverse current		
	Reverse saturation current	d)	Active current		
(vi)	Flip-flops can be used to design				
•	latches	b)	bounce -elimination switches		
	registers	d)	all of the above		
(vii)	Find the 2's complement of the number 1101101 -				
, ,			0111110		
a)	0101110		0010011		
	0110010 When an input signal A=11001 is applied to a NOT gate serially, its output signal				
(viii)	is represented as		2 ,,		
1	is rediesented as				

LIBRARY University Brainware University					
LIBO University	b) 00110				
Brahwar kata - 700	d) 11001				
e) 10101 An operational amplifier possesses (x) An operational amplifier possesses	 b) Very large input resistance and very small output resistance 				
An operational amplifier personal amplifier personal very large and very large and very small appropriate resistance.	d) Very small input resistance and very large output resistance.				
 very targe in a couput resistance output resistance very small input resistance and very small output resistance c) Convert decimal 153 to octal. Equivalent in o 	ctal will be				
output resistance output resistance in o octal. Equivalent in o	b) (331) ₈				
(x) Content	d) none of these				
a) (231) ₈	tempeistor called?				
c) (431)s (xi) What is the left hand section of a junction	(Tallistor				
	b) Collector				
a) base	d) Emitter				
c) depletion region (xii) The simplified form of Boolean expression	on $\overline{A} + A\overline{B}$ is				
(xii) The simplified form of Boolean Capresson					
	b) $A + \overline{B}$				
a) A+B	٠				
ol = 5	d) none of these				
(c) $\overline{A} + \overline{B}$	ed as				
(xiii) The fastest logic in logic families is indicate	b) TTL				
a) ECL	d) LSI				
c) CMOS	t resistance) =1k ohm .R2 (feedback				
(xiv) Consider the inverting OP-AMP with R1 (inputeresistance) =50k ohm and power supply voltage	$es \pm 12V$. Find the output voltage for an input				
resistance) = 50k offin and power supply voltage IV.					
	b) -12V				
a) -50V c) 50V	d) 12V				
(xv) Calculate how many AND gates are require	ed to realize $Y = CD + EF + G$				
a) 4	b) 5				
c) 3	d) 2				
(xvi) Calculate how many two input AND gates	and two input OR gates are required to				
realize					
Y = BD + CE + AB					
a) 1,1	b) 4,2				
c) 3,2	d) 2,3				
(xvii) In the operation of an NPN transistor, the e	lectrons cross which region?				
a) emitter region	b) The region where there is high depletic				
c) the region where there is low depletion	d) P type base region				
(xviii) The device which changes from serial data to parallel data is					
a) counter	b) multiplexer				
c) demultiplexer	d) flip-flop				
(xix) Select the two inputs of The NOR gate when output will be high					
a) 00	b) 10				
c) 01	d) 11				
(xx) When does the transistor act like an open switch?					
a) cut off region					
c) saturated region	b) Active regiond) None of these				
(xxi) The gates required to develop a half adder	are				
Of EA-UK gate and NOD and					
c) EX-OR gate and AND gate	b) EX-OR gate and OR gate				
8	d) Four NAND gates.				

xxii)	According to the property of minterm, calculate equal to 1 for K input variables?	culate how many combination will have				
а	•	b) 1				
	c) 2 d) 3) The output of a certain op-amp circuit changes by 20 V in 4 μs. Calculate slew rate					
	a) 50 V/µs	b) 500 mV/μs				
(c) 5 V/µs	d) 500 V/μs				
) Choose the following combinations of log					
	 a) One 4-input AND gate c) One 4-input AND gate, one OR gate d) Which of the following circuits consider circuits? 	b) One 4-input AND gate, one inverter d) One 4-input NAND gate, one inverter under the class of sequential logic				
	1. Full adder					
	2. Full subtractor					
	3. Half adder					
	4. J-K flip					
	5. Counter	a a second				
	a) 1 and 2	b) 2 and 3 d) 4 and 5				
1	c) 3 and 4 (xvi) Which of the following circuits consider	ler under the class of combinational logic				
(X)	circuits?					
	1. Full adder					
	2. Full subtractor					
	3. Half adder					
	4. J-K flip	•				
	5. Counter					
	a) 1 only	b) 3 and 4				
	1 4 and 5	d) 1,2 and 3				
(xxvii) Evaluate the required number of hal	b) $2^m - 1$				
	a) 2m – 1	d) 2m = 1				
	c) 2m + 1	several data inputs and allows only one of them				
(at a time to get through to the output	ll .				
	a) multiplexer	b) demultiplexer				
		d) receiver				
	(xxix) The output Q_n of a J-K flip-flop is 1.	it changes to 0 when a clock pulse is applied. the				
	input J _n and K _n are evaluated as					
	a) 0 and X	b) 1 and X d) X and 0				
c) X and 1 (xxx) Select the two inputs of the NAND gate if the output is low						
		b) 01				
	a) 00 c) 10	d) 11				

LIBRARY No.	Group-B					
Brainware University	wala choice Type Question)	3 x 10=30				
Barasat, Kolkata -700125	(Multiple Choice)					
the correct alternation	ve from the Johottan					
2. Choose the Contract	Choose the correct alternative from the following: To design the 4:1 MUX how many minimum basic gates are required b) 2 NOT gates, 3 AND gates a) 2 NOT gates, 4 AND gates					
dia 4:1 MUN b	ow many minimum b) 2 NOT gates, 3	AND gates				
(i) To design the same at 1 NOT gates, 3 AND gates, 4 AND	ates d) 2 NOT gates, 4	AND gates				
a) 1 NOT gates, 4 AND 8	ates are inputs of an S-R flip-flop	for creating a new				
c) 1 NOT garden is place	c) 1 NOT garden is placed between the imparts					
(ii) When an inventer is pass flip-flop which is known a	b) master-slave flip	p-flop				
1110-1101		•				
a) J-K flip-flop	d) D flip-flop the how many gates are required to imples b) 2 AND gates at gate b) 1 AND gates at	ment Y=AB +BC				
c) T flip-flop	e how many gates are required	vl 1 OR gate				
(iii) Choose the contest of QR	gate d) 1 AND gates at	vd 2 OR gate				
a) 2 AND gates and 2 OR	gate (1) 1 AND gates in	ment a full adder				
c) 1 AND gates and 7 continu	gate gate gate how many gates are required to imple b) 8 NAND gates					
(iv) Choose the correct of the	b) 8 NAND gates					
ay o NAND gates	d) 8 AND gates					
e) 9 AND gates	adecimal: $(1257.625)_8 = (?)_{16}$					
(v) Calculate the octains nex	adecimal: $(1257.625)_8 = (?)_{16}$ b) 2AF.CB8					
ALD ODG	W OAT CAO					
c) 2AF.CAS	d) $2AE.CA8$ as currents of 50 μA and 49.3 μA . The	input offset current				
(vi) A certain OP-amp has big	as currents of 50 far time					
: 2						
a) <font face="Times New</td><td>Roman, serif">700 b) 99.3 μΛ						
nA	d) None of these					
c) 7 nA	d) None of these	•				
(vii) To evaluate Y=						
•	_					
$\overline{A}B\overline{C} + \overline{A}\overline{B}C + \overline{A}BC + A$	$\overline{\mathcal{B}}C$:					
	b)					
a) $Y = \bar{A}B + \bar{B}C$	b) $Y = \bar{A}B + \bar{B}$	•				
-	d) cd					
c) $Y = \bar{A}B + C$	d) None of these					
(viii) To solve the (1983.5625)	$_{10} = (?)_{16}$					
•	b) 7BE.A					
a) 7BF.9	d) None of these					
c) 7BF.8	4.1 MIV only How many 4:1 MIX is re	eguired				
(ix) Convert a 16:1 MUX using	Convert a 16:1 MUX using 4:1 MUX only. How many 4:1 MUX is required					
a) 3	b) 4					
c) 5	d) 6					
(x) What is 1's complement a	and 2's of a number?					
a) 1's complement, one co	anyort to zero and b) 1's compleme	ent, one convert to zero and				
zero convert to one. 2's	complement = 1's zero convert t	o one. 2's complement = 1'				
+1	- 1	_				
c) 1's complement, one co						
· -		e				
zero convert to one. 2's	complement – 1.5 None of these	-				

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