BRAINWARE UNIVERSITY

Term End Examination 2022
Programme – B.Tech.(CSE)-2019
Course Name – VLSI
Course Code - OEC-701D
(Semester VII)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) VLSI technology identifies _____ to form integrated circuit.
a) Transistors b) switches
c) diodes d) buffers

(ii) Large-scale integration is defined by _____ number of transistors.
a) 10 to 500 b) 1 to 10
c) 20,000 to 1,000,000 d) 500 to 20,000

(iii) Choose, P-well doping concentration and depth will affect the _____
a) threshold voltage b) Vss
c) Vdd d) Vgs

(iv) State in which method regularity is used to reduce complexity.
a) random approach b) hierarchical approach
c) algorithmic approach d) semi-design approach

(v) Write the basic chemical reaction used for epitaxial growth of pure silicon.
a) hydrogen reduction of silicon tetrachloride. b) oxygen reduction of silicon tetrachloride.
c) hydrogen reduction of silicon pentachloride. d) oxygen reduction of silicon pentachloride.

(vi) Complete: In depletion mode, source and drain are connected by _____
a) insulating channel b) conducting channel
c) Vdd d) Vss

(vii) Cite that the photoresist layer is exposed to _____
a) Visible light b) Ultraviolet light
c) Infra red light d) LED

(viii) Express, in diffusion process of nMOS, _____ impurity is desired.
a) n type b) p type
c) np type d) none of the mentioned

(ix) Identify, if SIlicon-di-oxide is a good insulator.
a) correct b) not correct
c) sometimes d) never

(x) Conclude The drain current is varied by:

a) Gate to source voltage
b) Gate current
c) Source Voltage
d) None of the mentioned

(xi) Deduce the logical low voltage (logic 0) or negative voltage on the gate of p-MOSFET forms _____

a) Channel of negative carriers
b) Channel is not formed
c) Channel is clipped
d) Channel of positive carriers

(xii) Choose, which MOSFET is generally connected to the Vdd in a circuit?

a) PMOS
b) NMOS
c) CMOS
d) DMOS

(xiii) Conclude, the current through the n-MOS transistor will flow when:

a) Vgs > Vtreshold, Vds=0
b) Vgd < Vtreshold, Vds=0
c) Vgs > Vtreshold, Vds>0
d) Vgd > Vtreshold, Vds<0

(xiv) Report the switching threshold voltage VTH for an ideal inverter is equal to:

a) (VDD-VOL)/2
b) VDD
c) (VDD)/2
d) 0

(xv) Report the electrical equivalent component for MOS structure is:

a) Resistor
b) Capacitor
c) Inductor
d) Switch

Group-B

(Short Answer Type Questions) 3 x 5=15

2. Report functions of SiO2. (3)
3. Examine Vapor Phase Epitaxy. (3)
4. With circuit diagram of CMOS NAND gate, describe output formation of the truth table, for each input combination. (3)
5. What are the different types of VLSI Chips? (3)
6. Construct CMOS full adder by any two different ways. (3)

OR

Rewrite Full custom and Semi-custom design. (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Identify Analog & Digital VLSI chips, General purpose, ASIC, PLA and FPGA. (5)
8. Illustrate Ion Implantation. (5)
9. Construct the diagrams for every step in CMOS fabrication. (5)
10. Illustrate Stick diagram. (5)
11. Analyze the drawing of 3-input CMOS NAND & NOR Gates and their truth tables with explanation of how each output is generated. (5)
12. Criticize Full custom and Semi-custom design. (5)

OR

Justify FPGA building block architectures. (5)

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