BRAINWARE UNIVERSITY

Term End Examination 2022
Programme – M.Tech.-RA-2022
Course Name – Electronics in Robotic Technology
Course Code - PEC-MIRA102B
(Semester I)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Select the two inputs of the NAND gate if the output is low
a) 0 b) 1
c) 10 d) 11

(ii) Select the decimal equivalent of hex number 1A53
a) 6793 b) 6739
c) 6973 d) 6379

(iii) A FET is better chopper than a BJT because it has
a) Low offset voltage b) High input voltage
c) High input current d) High series ON resistance

(iv) A FET consists of a
a) Source b) Drain
c) Gate d) All of these

(v) In a JFET, drain current is maximum when VGS is
a) Zero b) Negative
c) Positive d) Equal to pinch-off voltage

(vi) In the operation of an NPN transistor, the electrons cross which region?
a) emitter region b) The region where there is high depletion
c) the region where there is low depletion d) P type base region

(vii) According to the property of minterm, calculate how many combination will have value equal to 1 for K input variables?
a) 0 b) 1
c) 2 d) 3

(viii) How many flip-flops are required to construct mod 30 counter
a) 5 b) 6

c) 4 d) 8

(ix) For the operation of enhancement- only N-channel MOSFET, value of gate voltage has to be

a) High positive b) High negative
c) Low positive d) Zero

(x) Calculate how many two input AND gates and two input OR gates are required to realize Y = BD+CE+AB

a) 1, 1 b) 4, 2
c) 3, 2 d) 2, 3

(xi) Calculate minimum number of two input NAND gates required to realize XNOR gate

a) 3 b) 4
c) 5 d) 6

(xii) Let the input of a subtractor is A and B; then calculate the output if A = B.

a) 0 b) 1
c) A d) B

(xiii) Choose a logic circuit that accepts several data inputs and allows only one of them at a time to get through to the output

a) multiplexer b) demultiplexer
c) transmitter d) receiver

(xiv) Early effect in a transistor is known as

a) Zener breakdown b) Avalanche breakdown
c) Thermal breakdown d) Reduction in width of base or base narrowing

(xv) How many AND, OR and EXOR gates are required to design a full adder?

a) 1, 2, 2 b) 2, 1, 2
c) 3, 1, 2 d) 4, 0, 1

Group-B
(Short Answer Type Questions) 3 x 5=15

2. State and explain De-Morgans Law. (3)
3. Construct a full adder circuit using a 3 to 8 line decoder. (3)
4. Construct Ex-OR gate using NAND gates only (3)
5. Simplify the following expression using K-map method: F= m (7,9,10,11,12,13,14,15) (3)
6. Write a short note on the Master slave JK flip flop. (3)

OR

Design a JK Flip Flop using a D Flip Flop (3)

Group-C
(Long Answer Type Questions) 5 x 6=30

7. Explain how RS flip-flop can be obtained by using NOR gates (5)
8. Explain the use of an OPAMP as summing amplifier. (5)
9. Explain the construction of J-K flip flop using S-R flip flop (5)
10. Describe OP Amp as a differentiator (5)
11. Calculate the output voltage for the summing amplifier circuit using OPAMP. Given V1=0.2V,V2=2V,V3=1V and R1=5KΩ, R2=20KΩ, R3=50KΩ and Rf=30KΩ, where notations carry the usual meanings (5)

OR

Construct and explain the full adder circuit using two half adder circuit through a block (5)

diagram.

12. The transfer characteristic of an n-channel JFET is given, with usual symbols, by I_{DS} = $I_{DSS}(1 - V_{GS}/V_P)^2$. Evaluate an expression for g_m from the above parabolic equation of the transfer characteristic, show how g_m varies with V_{GS} and I_{DS}. (5)

OR

Distinguish between Synchronous and Asynchronous counters. (5)

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