BRAINWARE UNIVERSITY

Term End Examination 2025-2026
Programme – B.Tech.(CSE)-DS-2024/B.Tech.(CSE)-CYS-2024/B.Tech.(CSE)-CYS-2025/B.Tech.(CSE)-DS-2025
Course Name – Applied Digital Logic Design
Course Code - BES00018
(Semester II)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A
(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Select the binary equivalent of the decimal number 368
   a) 101110000 b) 110110000
   c) 111010000 d) 111100000

(ii) Select the decimal equivalent of the octal number 140
   a) 96 b) 86
   c) 90 d) None of these

(iii) Select the Octal equivalent number of binary number 110001010
   a) 512 b) 612
   c) 432 d) 430

(iv) Select the derived gate that can be used as a controlled inverter.
   a) AND b) OR
   c) NAND d) XOR

(v) Select the code where consecutive numbers differ in only one bit
   a) BCD b) Binary
   c) Grey d) XS-3

(vi) Memorize the IC number for NAND Gate
   a) 7486 b) 7400
   c) 7432 d) 7402

(vii) Choose the gate which is placed between clock input and the input of AND gate to convert a positive level triggered flip – flop to a negative level triggered flip – flop
   a) NOR gate b) NOT gate
   c) Buffer d) NAND gate

(viii) Identify the group of 1s present in 8 cells of a K – map called.
   a) Pair b) Quad

c) Octet
d) Octave

(ix) Identify the law by which we can write "X + XY = X"

a) Consensus law
b) Distributive law
c) Duality law
d) Absorption law

(x) Choose how many 1024 * 1 RAM chips are required to construct a 1024 * 8 memory system

a) 4
b) 6
c) 8
d) 12

(xi) Choose the correct option-A digital circuit that can store only one bit is a representation of

a) Register
b) NOR gate
c) Flip-flop
d) XOR gate

(xii) Identify the correct option - output will be a LOW for any case when one or more inputs are zero

a) OR gate
b) NOR gate
c) NOT gate
d) AND gate

(xiii) Predict the correct answer: "In Boolean algebra, the bar sign (-) indicates ....."

a) OR operation
b) AND operation
c) NOT operation
d) None of the these

(xiv) Choose the main advantage of JK flip-flop over SR flip-flop.

a) Simpler circuit.
b) No invalid state.
c) Faster response.
d) Lower power consumption.

(xv) Determine which register converts serial data to parallel data.

a) SISO.
b) SIPO.
c) PIPO.
d) PISO.

Group-B

(Short Answer Type Questions) 3 x 5=15

2. State Boolean expression, truth table, and logical symbol of NAND gate. Realized OR gate by NAND (3)

3. Discuss De-Morgan's Law. (3)

4. Illustrate the difference between JK Flip Flop and SR Flip Flop. (3)

5. Apply Boolean algebra to prove the expression $A + \overline{A} \cdot B = A + B$ (3)

6. Summarize the operation of OR gate using 2:1 MUX (3)

OR

Summarize the operation of AND gate using 2:1 MUX (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Estimate the simplified boolean expression of the following expression using K-MAP (5)

   $F=\Pi(0,3,6,7)$

8. Illustrate D flip-flop with its truth table, circuit diagram and working principle (5)

9. Construct 8:1 multiplexer using 4:1 multiplexer and OR gate. (5)

10. Reproduce Y=AB+AC'+BC in Canonical SOP format and develop the corresponding truth table. (5)

11. Identify the simplified expression for the logic expression (5)

$$f(A, B, C, D) = \Pi M(4, 5, 6, 7, 8, 12) \cdot d(1, 2, 3, 9, 11, 14)$$

12. Explain the conversion technique of JK flip-flop to D flip-flop. (5)

OR

Explain the working principle of synchronous counter. (5)

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