35033-37971-44348-44376

BRAINWARE UNIVERSITY

Term End Examination 2025-2026
Programme – BCA-Hons-2024/BCA(MAWT)-Hons-2024/BCA-Hons-2025/BCA(MAWT)-Hons-2025
Course Name – Computer Organization
Course Code - VAC00016
(Semester II)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A
(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) In register transfer operations, the symbol "←" is used to represent:
- a) Logical AND operation
- b) Assignment of data from one register to another
- c) Memory addressing
- d) Arithmetic addition

(ii) Which logic micro-operation produces an output of 1 only when the inputs are different?
- a) AND
- b) OR
- c) XOR
- d) NOT

(iii) The control memory is usually implemented using:
- a) RAM
- b) ROM
- c) Cache Register
- d) File

(iv) The process of selecting the next microinstruction address is called:
- a) Address sequencing
- b) Instruction decoding
- c) Memory mapping
- d) Pipelining

(v) A hardwired control unit is typically-
- a) Faster than a microprogrammed unit
- b) Slower than a microprogrammed unit
- c) More flexible than a microprogrammed unit
- d) Based on software execution

(vi) What is the 2's complement of the binary number 1010?
- a) 101
- b) 1011
- c) 1110
- d) 110

(vii) Given two binary numbers 1101 and 0110, what is their sum?
- a) 1001
- b) 1011
- c) 10011
- d) 11101

(viii) What is the result of adding 0110 (BCD) and 0101 (BCD)?

a) 1011 1100 0001 0001 (BCD)
b) 1011, which would need a correction to 0001 0001(BCD)
c) 0001(BCD)
d) 1110(BCD), which would need a correction to 0001 0001(BCD)

(ix) In a non-restoring division algorithm, what happens when a subtraction results in a negative remainder?

a) The division operation is terminated
b) The remainder is restored by adding the divisor.
c) The quotient bit is set to 0
d) The divisor is added to the negative remainder, and the next quotient bit is set to 0

(x) Identify the memory that stores microinstructions in a microprogrammed control unit.

a) Main Memory
b) Cache Memory
c) Control Memory
d) Virtual Memory

(xi) Select the component that generates the address of the next microinstruction.

a) Address Sequencer
b) ALU
c) Program Counter
d) Decoder

(xii) Which group of registers is used to store general-purpose data?

a) Cache Registers
b) General Register Organization
c) Control Registers
d) Special Registers

(xiii) What are the advantages and disadvantages of using programmed I/O compared to interrupt-driven I/O?

a) Programmed I/O is faster.
b) Programmed I/O wastes CPU time, interrupt-driven I/O is more efficient.
c) Interrupt-driven I/O is simpler.
d) They are identical.

(xiv) What is the main goal of pipelining in computer architecture?

a) Reduce power consumption
b) Increase memory size
c) Improve instruction throughput
d) Simplify instruction decoding

(xv) What is a crossbar switch in a multiprocessor system?

a) A bus-based interconnection
b) A ring-based interconnection
c) A hypercube interconnection
d) A switch that allows any processor to connect to any memory module

Group-B

(Short Answer Type Questions) 3 x 5=15

2. What are memory reference instructions? List any two with their functions. (3)
3. Explain the concept of "address sequencing" in microprogrammed control. (3)
4. Briefly explain the difference between a zero-address and a one-address instruction format. (3)
5. Show how the "indirect addressing mode" would access an operand. (3)
6. Briefly outline the steps involved in Booth's multiplication algorithm. (3)

OR

Explain how floating-point addition is performed, highlighting the key steps. (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Explain the concept of "register transfer language" (RTL) and provide examples of how it can be used to describe data movement between registers. (5)
8. Explain the instruction cycle of a basic computer, including the fetch, decode, and execute phases. (5)
9. Design a basic instruction format that includes fields for opcode, register operands, and addressing mode. Show how a specific instruction, such as "LOAD R1, address," can be (5)

represented in this format using different addressing modes.

10. Implement a simple ALU with control signals to perform arithmetic and logical operations. Demonstrate how the control signals are used to select the desired operation for a specific instruction. (5)
11. The evolution of computer architecture has led to two dominant paradigms: Complex Instruction Set Computing (CISC) and Reduced Instruction Set Computing (RISC). (a) Analyze the fundamental architectural differences between CISC and RISC, focusing on their instruction set complexity, addressing modes, and pipeline efficiency. (b) Subsequently, evaluate the trade-offs associated with each architecture in terms of performance, power consumption, and suitability for different application domains. Justify which architecture, in your opinion, offers a more advantageous design philosophy for modern computing needs, and explain the reasoning behind your choice. (5)
12. Multiply 12 (multiplicand) by -5 (multiplier) using Booth's algorithm. Show all steps. What is the advantage of Booth's algorithm over standard multiplication for these numbers? (5)

OR

Calculate the product of -6 (multiplicand) and -3 (multiplier) using Booth's algorithm. Document each step. Explain the role of the extra bit in Booth's algorithm. (5)

****