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BRAINWARE UNIVERSITY

Term End Examination 2025-2026
Programme – B.Tech.(CSE)-AIML-2021/B.Tech.(CSE)-DS-2021/B.Tech.(CSE)-AIML-2022/B.Tech.(CSE)-DS-2022
Course Name – VLSI Design
Course Code - OEC-CSM801B/OEC-CSD801B
(Semester VIII)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Identify the two primary levels of design abstraction used in VLSI design.
   a) Behavioral and structural
   b) Logical and physical
   c) Sequential and combinational
   d) Analog and digital

(ii) List some common design tools used in VLSI design.
   a) Logic synthesis tools, place and route tools, layout editors
   b) Hammers, screwdrivers, wrenches
   c) Paintbrushes, pencils, erasers
   d) Not mentioned

(iii) Identify the main advantage of using a Hardware Description Language (HDL) in VLSI design.
   a) It allows designers to describe and simulate a circuit's behavior at a high level of abstraction.
   b) It allows designers to physically construct a circuit using individual components.
   c) It allows designers to test a circuit's performance under various conditions.
   d) It allows designers to program the behavior of a circuit using software.

(iv) Classify the types of semiconductor materials used in Silicon technology.
   a) Intrinsic and Extrinsic
   b) Conductors and Insulators
   c) N-type and P-type
   d) Metals and Alloys

(v) Recall the main reason why CMOS is preferred over NMOS.
   a) Lower power consumption
   b) Higher noise margin
   c) Less area requirement
   d) Lower propagation delay

(vi) Identify the logic function implemented by a CMOS full adder.
   a) Addition
   b) Subtraction
   c) Multiplication
   d) Division

(vii) Summarize the advantages of edge-triggered flip-flops.

a) Less power consumption
b) Better synchronization
c) Lower latency
d) Faster response

(viii) Calculate the power dissipation of a CMOS inverter with given parameters.

a) $P = IV$
b) $P = fCV^2$
c) $P = V^2/R$
d) $P = I^2R$

(ix) Predict the behavior of a CMOS inverter under different input voltages.

a) Output follows input
b) Acts as a switch
c) Works as a buffer
d) Holds intermediate state

(x) List the main design approaches in VLSI.

a) Full Custom Design
b) Semi-Custom Design
c) Hybrid Design
d) ASIC Design

(xi) Outline the advantages of FPGA over ASIC.

a) Reprogrammability
b) Lower Cost
c) Faster Speed
d) Fixed Functionality

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(xii) Perform a comparison between ASIC and FPGA performance.

a) ASIC is Faster
b) FPGA is Faster
c) Both are Same
d) Depends on Application

(xiii) Model a CMOS-based XOR gate using NAND gates.

a) 3 NAND gates
b) 4 NAND gates
c) 5 NAND gates
d) 6 NAND gates

(xiv) Examine what is the purpose of the ion implantation process:

a) Collect the implanted ions
b) Relate the implantation dosage
c) Judge the implantation energy
d) Change the doping concentration

(xv) Choose the act of depositing a thin layer of silicon onto a silicon wafer

a) Cleaning
b) Etching
c) Epitaxial Deposition
d) Photo-lithography

Group-B

(Short Answer Type Questions) 3 x 5=15

2. Illustrate the oxidation process in semiconductor manufacturing and discuss its importance. (3)
3. Discuss the role of photolithography in VLSI fabrication and differentiate between positive and negative photoresists. (3)
4. Describe Moor's Law. (3)
5. Identify the basic idea behind MSI. (3)
6. Classify the different types of CMOS logic circuits and justify their advantages over traditional MOS logic. (3)

OR

Analyze the working principle of a CMOS inverter and illustrate its characteristics with a proper diagram. (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Explain a detailed step-by-step plan for the photolithography process in VLSI fabrication and explain how positive and negative photoresists influence pattern formation (5)
8. Evaluate the impact of power consumption and propagation delay in CMOS logic design, suggesting methods to optimize them. (5)
9. Simplify the process of FPGA logic synthesis and implementation. (5)
10. Associate the role of standard cell libraries with semi-custom design automation. (5)
11. Describe the differences between Full-Custom and Semi-Custom VLSI design methodologies. Provide advantages, disadvantages, and typical applications of each. (5)

12. Illustrate the role of epitaxial deposition in semiconductor fabrication with a detailed diagram. (5)

OR

Differentiate between ion implantation and diffusion techniques in semiconductor doping. (5)

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