BRAINWARE UNIVERSITY

Term End Examination 2022
Programme – B.Tech.(CSE)-AIML-2021/B.Tech.(CSE)-DS-2021
Course Name – Computer Organization and Architecture
Course Code - PCC-CSM301/PCC-CSD301
(Semester III)

Full Marks : 60   **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A
(Multiple Choice Type Question)   1 x 15=15

1. *Choose the correct alternative from the following :*

(i)   Convert the binary number (1111000011110000) to hexadecimal number

    a) 1010   b) F0F0
    c) 7070   d) 5050

(ii) The situation wherein the data of operands are not available is called _____ Write the correct answer.

    a) Data hazard   b) Stock
    c) Deadlock   d) Structural hazard

(iii) Select the format which is usually used to store data

    a) Hexadecimal   b) Octal
    c) Binary   d) Decimal

(iv) Select which of the following is a universal logic gate? .

    a) OR   b) AND
    c) XOR   d) NAND

(v)   The fetch and execution cycles are interleaved with the help of _____. Write the correct answer.

    a) Modification in processor architecture   b) Clock
    c) Special unit   d) Control unit

(vi) Apply signed-magnitude binary division and find the result if the dividend is (11100)2 and divisor is (10011)2

    a) 10100   b) 100
    c) 11001   d) 1100

(vii) What is the formula for Hit Ratio identify?

    a) Hit/(Hit + Miss)   b) Miss/(Hit + Miss)
    c) (Hit + Miss)/Miss   d) (Hit + Miss)/Hit

(viii) Write the number which is numerically equal to (100110)2

a) (46)8   b) (2A2)H
c) (36)10   d) (26)10

(ix) Auxillary memory access time is generally _____ times that of the main memory identify?

a) 10   b) 100
c) 1000   d) 10000

(x) Define ASCII

a) American Stable Code For International   b) American Standard Case For Institutional
   Interchange   Interchange
c) American Standard Code For Interchange   d) American Standard Code For Information
   Information   Interchange

(xi) Judge the memory implemented using the semiconductor chips is _____

a) Cache   b) Main
c) Secondary   d) Registers

(xii) Which of the following is independent of the address bus devise?

a) Secondary memory   b) Main memory
c) Onboard memory   d) Cache memory

(xiii) If M denotes the number of memory locations and N denotes the word size, then evaluate the storage capacity is _____

a) $M*N$ b) $M+N$
c) $2M+N$ d) $2M-N$

(xiv) Select which of the following is/are type of pipelining

a) instruction   b) arithmetic
c) Both of these   d) none of these

(xv) Write which of the following is the lowest in the computer memory hierarchy?

a) Cache   b) RAM
c) Secondary memory   d) CPU registers

Group-B
(Short Answer Type Questions)

3 x 5=15

2. Explain Instruction Cycle with diagram.   (3)
3. Explain the functions of different input/output instructions in a basic computer.   (3)
4. Explain the differences between Latches and Flip-flops.   (3)
5. Define Basic Terminology of Computer Organization and Architecture.   (3)
6. Explain multiple-bus structure with advantages and disadvantages.   (3)

OR

What is an Addressing Mode?   (3)

Group-C
(Long Answer Type Questions)

5 x 6=30

7. Explain cache memory   (5)
8. State the difference between computer organization and computer architecture.   (5)
9. Explain propagation delay of Ripple Carry Adder and how it can be reduced in Carry Look (5)
   Ahead adder, explain with suitable block diagram
10. Explain the memory hierarchy pyramid   (5)
11. Explain Memory management unit(MMU)   (5)
12. Briefly explain different types of interrupts   (5)

OR

Explain pipelining and its different types.   (5)

Page 2 of 3

****