BRAINWARE UNIVERSITY

Term End Examination 2022
Programme – B.Tech.(RA)-2021
Course Name – Digital System Design
Course Code - PCC-ECR302
(Semester III)

Time : 2:30 Hours

Full Marks : 60

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Select the binary equivalent of the decimal number 368 - .

a) 101110000 b) 110110000
c) 111010000 d) 111100000

(ii) The output of a logic gate is 1 when all its inputs are at logic 0. Identify the gate(s)-

a) a NAND or an EX-OR b) an OR or an EX-NOR
c) an AND or an EX-OR d) a NOR or an EX-NOR

(iii) Select the two inputs of The NOR gate when output will be high

a) 0 b) 1
c) 10 d) 11

(iv) When an input signal A=11001 is applied to a NOT gate serially, its output signal is represented as

a) 111 b) 110
c) 10101 d) 11001

(v) The binary equivalent of (FA)16 is indicated as

a) 1010 1111 b) 1111 1010
c) 10110011 d) none of these

(vi) Convert (0.345)10 into an octal number

a) (0.16050)8 b) (0.26050)8
c) (0.19450)8 d) (0.24040)8

(vii) How many flip flops are required to construct a decade counter

a) 10 b) 3
c) 4 d) 2

(viii) The device which changes from serial data to parallel data is

a) counter b) multiplexer

c) demultiplexer
d) flip-flop

(ix) Karnaugh map is chosen for the purpose of
a) Reducing the electronic circuits used
b) To map the given Boolean logic function
c) To minimize the terms in a Boolean expression
d) To maximize the terms of a given a Boolean expression

(x) Calculate minimum number of two input NAND gates required to realize XOR gate
a) 3
b) 4
c) 5
d) 6

(xi) Calculate How many NAND circuits are contained in a 7400 NAND IC?
a) 2
b) 4
c) 8
d) 6

(xii) In a master-slave J-K flip-flop, evaluate the state Qn+1 of the flip-flop after the clock pulse when J=K=1
a) 0
b) 1
c) Qn
d) Qn'

(xiii) Evaluate the output when a flip-flop is set
a) Q=0 , Q' = 0
b) Q=1 , Q' = 0
c) Q=0 , Q' = 1
d) Q=1 , Q' = 1

(xiv) How many NOT gates are required for the construction of a 4-to-1 multiplexer?
a) 3
b) 4
c) 2
d) 5

(xv) A mod-5 synchronous counter is designed using J-K flip-flops. the number of counts it will skip is
a) 2
b) 3
c) 5
d) 10

Group-B
(Short Answer Type Questions) 3 x 5=15

2. Write down the Boolean expression of output Y of EX-OR gate and show how it can be realized by using AND, OR and NOT gates. Present the logic symbol of EX-OR gate (3)
3. Construct Ex-OR gate using NAND gates only (3)
4. Construct a full adder using 8:1 multiplexer. (3)
5. Simplify the following expression using K-map method: F= Æ©m (7,9,10,11,12,13,14,15) (3)
6. Design Binary to Gray code converter using logic gates (3)

OR

Write a short note on the Master slave JK flip flop. (3)

Group-C
(Long Answer Type Questions) 5 x 6=30

7. Describe the salient features of BCD, Excess-3 Code and Gray Codes with examples. (5)
8. Illustrate NOR gate and demonstrate the action of NOR gate as Universal gate. (5)
9. Illustrate NAND gate and demonstrate the action of NOR gate as Universal gate. (5)
10. Explain how RS flip-flop can be obtained by using NOR gates (5)
11. Explain the design of a MOD 14 asynchronous UP/DOWN counter with JK flip flop. (5)
12. Distinguish between Synchronous and Asynchronous counters. (5)

OR

Discriminates between combinational circuit and sequential circuit. (5)