BRAINWARE UNIVERSITY

Term End Examination 2023-2024
Programme – B.Sc.(ANCS)-Hons-2022
Course Name – Computer Organization and Architecture
Course Code - GEEC401
(Semester IV)

Full Marks : 60 **Time : 2:30 Hours**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A

(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Identify the correct choices for the definition of computer architecture

a) set of categories and methods that specify the functioning, organization, and implementation of computer systems
b) set of principles and methods that specify the functioning, organization, and implementation of computer systems
c) set of functions and methods that specify the functioning, organization, and implementation of computer systems
d) None of the mentioned

(ii) If an exception is raised and the succeeding instructions are executed completely, then the processor is generalized to have _____

a) Generation word
b) Exception handling
c) Imprecise exceptions
d) None of the mentioned

(iii) To reduce the memory access time we generally classify to make use of _____

a) SDRAM's
b) Heaps
c) Cache's
d) Higher capacity RAM's

(iv) The ALU associate to make use of _____ to store the intermediate results.

a) Accumulators
b) Registers
c) Heap
d) Stack

(v) CPU associate with

a) main memory and ALU
b) main memory, ALU and control unit
c) cache memory, ALU and control unit
d) ALU, control unit and registers.

(vi) In CISC architecture,represent instructions typically perform:

a) Simple operations
b) Single operations
c) Multiple operations
d) No operations

(vii) Select,which of the following is a disadvantage of CISC architecture?

a) Small code size
b) Simplified instruction decoding
c) Increased complexity of hardware
d) Better performance

(viii) Identify,which of the following is true about DMA?

a) CPU is involved in every data transfer.
b) DMA is slower compared to Interrupt Driven I/O.
c) DMA reduces CPU involvement in data transfer.
d) DMA is only used for secondary storage devices.

(ix) Write DMA transfers are typically used for:
a) Bulk data transfers
b) Real-time processing
c) Interactive processing
d) Arithmetic operations

(x) Choose the following is not a type of DMA transfer mode.
a) Burst mode
b) Cycle-stealing mode
c) Demand mode
d) Parallel mode

(xi) Indicate, which mode of DMA transfer is suitable for high-speed data transfers?
a) Burst mode
b) Cycle-stealing mode
c) Demand mode
d) Parallel mode

(xii) Choose the following is the fastest type of memory.
a) Cache memory
b) Secondary memory
c) Main memory
d) Virtual memory

(xiii) Write down the main purpose of cache memory.
a) To store frequently accessed data
b) To increase the capacity of memory
c) To provide a permanent storage solution
d) To replace main memory

(xiv) Which stage of the instruction execution cycle involves writing the result back to the register file?
a) Fetch
b) Decode
c) Execute
d) Writeback

(xv) If a program takes 200 seconds to execute without optimization and 50 seconds to execute with optimization, estimate the speedup achieved.
a) 2
b) 4
c) 0.25
d) 150

Group-B

(Short Answer Type Questions) 3 x 5=15

2. Briefly discuss about the maximum number of 0-address, 1-address and 2-address instructions if the instruction size is of 32-bit and 10-bit address field. (3)

3. Explain the stages of instruction execution in a RISC computer. (3)

4. Suppose a 30 GB hard-disk is to be manufactured. If the technology used to manufacture the disks allows 1024-byte sectors, 2048-sector tracks and 4096-track platters. Calculate, how many platters are required? (3)

5. A hierarchical cache-main memory subsystem has the following specifications: (i) Cache access time of 160 ns (ii) main memory access time of 960 n (iii) hit ratio of cache memory is 0.9. Calculate the following: (a) Average access time of the memory system. (b) Efficiency of the memory system. (3)

6. Illustrate digital logic. (3)

OR

Illustrate the basics of a computer. (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Given a non-pipelined processor with 15 ns clock period. Calculate how many stages of pipelined version of the processor are required to achieve a clock period of 4 ns? Assume that the interface latch has delay of 0.5 ns. (5)

8. Explain the fundamentals of digital logic and its significance in computer systems. (5)

9. Mention the differences between vectored and non-vectored interrupt. (5)

10. *A 50 MHz processor was used to execute a program with the following instruction mix and clock cycle counts:* (5)

Instruction type	*Instruction count*	*Clock cycle count*
Integer arithmetic	*50000*	*1*
Data transfer	*35000*	*2*
Floating point arithmetic	*20000*	*2*
Branch	*6000*	*3*

Calculate the effective CPI, MIPS rate and execution time for this program.

11. Show the addressing for program and data, assuming von Neumann architecture for storing the following program: (a) Assume that a program has a length of 2048 bytes and the program starts from an address 0. (b) The input data size is 512 bytes and stores from 3000. (c) The results of 30 bytes generated after program execution are stored at address 4000. (5)

12. Explain General Purpose Register Organization in CPU. (5)

OR

Compare RISC and CISC architecture in CPU organizations. (5)

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