BRAINWARE UNIVERSITY

Term End Examination 2018 - 19

Programme – Bachelor of Computer Applications

Course Name – Computer Architecture & Organization

Course Code – BCAC203 / BCA203

(Semester – 2)

Time allotted: 3 Hours **Full Marks : 70**

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group –A

(Multiple Choice Type Questions) 10 x 1 = 10

1. *Choose the correct alternative from the following*

(i) Elementary components of a single CMOS SRAM cell are constructed with

a. Nine capacitors
b. Six transistors
c. Two transistors and two inverters
d. One transistor with a capacitor

(ii) A single DRAM cell is constructed with

a. six transistors.
b. two transistors and one capacitor.
c. one capacitor, one transistor.
d. one capacitor.

(iii) Format of IEEE 754 double precision is divided with

a. 64-bit format in which 11-bit is for biased exponent E', 52-bit for mantissa M and 1-bit for the sign of the number.
b. 64-bit format in which 52 -bit is for biased exponent E', 11-bit for mantissa M and 1-bit for the sign of the number.
c. 32-bit format, in which 8-bit is for exponent, 23-bit is for mantissa, 1 bit to represent the sign bit.
d. 32-bit format, in which 23-bit is for exponent, 8-bit is for mantissa, 1 bit to represent the sign bit.

(iv) A ROM type memory chip of size 1K X 16 will have

a. 10 bit address bus and 16 bit bidirectional data bus
b. 1KB address bus and 2^4 bit bidirectional data bus
c. 1K bit address bus and 8 bit unidirectional data bus
d. 10 bit address bus and 16 bit unidirectional data bus

(v) Performance of a cache memory is measured by

a. a quantity called 'hit ratio'
b. a quantity called 'miss ratio'
c. a probability
d. booth's algorithm

(vi) The instruction does not have any operand field in

a. Auto-increment mode
b. Auto-decrement mode
c. Stack mode
d. Register mode

(vii) Data hazards may occur in a pipeline, when

a. When two instruction use same RAM
b. When two instructions use data from the same register.
c. When two instructions use same data
d. When two instructions use data from different registers

(viii) Main advantages of associative memory is

a. It is cheap
b. it is suitable to store data rapidly
c. it built with semiconductors
d. it is suitable for parallel searches due to its organization

(ix) Carry look ahead adder works faster than other adders, because

a. it adds more than two numbers.
b. it adds two numbers serially.
c. it adds two numbers without depending on the carry bits from the previous stages.
d. it adds only carry bits.

(x) What are the use of general purpose register is

a. To store general input bits and intermediate data bits
b. To store data and intermediate results during the execution of a program
c. To store cache elements and hit ratio information
d. To store carry bits, and propagate the bits to carry flag register

Group – B

(Short Answer Type Questions) 3 x 5 = 15

Answer any *three* from the following

2. How can you differentiate between paging and segmentation. 5

3. Why is frequent refreshing necessary for DRAM type memory? Describe a typical DRAM memory cell with necessary logic diagram. 2+3

4. Compare various Lengths of Instructions through proper arithmetic Expression. 5

5. Compare Structural Hazards and Data Hazards with suitable examples. 5

6. Explain step by step procedure for I/O Interface (Interrupt and DMA Mode). 5

Group – C

(Long Answer Type Questions) 3 x 15 = 45

Answer any *three* from the following

7. (a) Explain the concept of Locality of Reference in brief. What is Spatial and Temporal reference? 5+3

   (b) Represent number 210.25_{10} in IEEE 754 floating point format. 7

8. (a) Construct a n-line common bus system with MUX, for register transfer four registers D,C,B & A each of n-bits have been used The common bus is used to transfer a register's content to other register or memory at a single time. The bus consists of four 4 X 1 multiplexers each with four data inputs, and two data inputs as two selection lines (S_0 and S_1). 7

   (b) A three level memory system has cache access time of 3 nsec, and disk access time of 50 nsec. It has a cache hit ratio of 0.18 and the main memory hit ratio of 0.7. What should be the main memory access time to achieve an overall access time of 16 nsec? 8

9. (a) Construct a memory of capacity 1024 X 4 (or 1K X 4, with RAM of size 512 X 4 and ROM of size 512 X 4. 8

   (b) Construct a general 4 bit basic logical operator with necessary block diagram. 7

10. (a) Construct a 1K X 16 large RAM type memory with 256 X 8 RAM chips. 10

	(b)	Describe the working principle a typical magnetic memory with necessary diagrams.	5
11.	(a)	A memory sub system has with a hierarchical cache memory-main has cache access time of 60 nsec., main memory access time of 120 nsec. and an overall hit ratio of 0.12. Calculate efficiency of the memory system.	7
	(b)	A three level memory system having cache access time of 3 nsec, and disk access time of 70 nsec, it has a cache hit ratio of 0.16 and the main memory hit ratio of 0.7. what should be the main memory access time to achieve an overall access time of 16 nsec?	8