BRAINWARE UNIVERSITY

Term End Examination 2023
Programme – BCA-2019/BCA-2020/BCA-2021
Course Name – Computer Organization and Architecture
Course Code - BCAC202
(Semester II)

Time : 2:30 Hours

Full Marks : 60

[The figure in the margin indicates full marks. Candidates are required to give their answers in their own words as far as practicable.]

Group-A
(Multiple Choice Type Question) 1 x 15=15

1. *Choose the correct alternative from the following :*

(i) Select the correct one, In a generic microprocessor instruction cycle time is

a) Shorter than machine cycle time
b) Larger than machine cycle time
c) Ten times the machine cycle time
d) Exactly the same as the machine cycle time

(ii) Indicate that the stack pointer in the microprocessor is a

a) 16 bit register that point to stack memory locations
b) 32 bit accumulator
c) memory location in the stack
d) flag register used for the stack

(iii) Select, The Micro program is

a) The name of source program in micro computers
b) The set of instructions indicating the primitive operations in a system
c) Primitive form of macros used in assembly language programming
d) Program of very small size

(iv) Select, If we use 3 bits in the instruction word to indicate if an index register is to be used and if necessary, which one is to be used, then the number of index registers to be used in the machine will be

a) 3
b) 6
c) 5
d) 8

(v) Select, in the absolute addressing mod

a) Operand is inside the instruction
b) Address of the operand is outside the instruction
c) Register containing the address of the operand is specified inside the instruction
d) Location of the operand is implicit.

(vi) Identify the addressing mode used in an instruction of the form ADD X, Y, is

a) absolute
b) immediate
c) Relative
d) indirect

(vii) State the ability to temporarily halt the CPU and use this time to send information on buses is called

a) Direct memory access
b) Vectoring the interrupt
c) System Interrupt
d) Cycle stealing

(viii) Identify Pseudo-instructions are

a) Assembler directives
b) Instructions in any program that have corresponding machine code instruction
c) Instruction in any program whose absence will not change the output for any input
d) None of these

(ix) Identify the addressing mode used in the instruction PUSH B is

a) Direct
b) Register
c) Register indirect
d) Index

(x) State the CPU of a Computer takes instruction from the memory and executes them. This process is called

a) Load cycle
b) Time sequence
c) Fetch-execute cycle
d) Incognito mode in a browser

(xi) Choose the reason for the implementation of the cache memory is _____

a) To increase the internal memory of the system
b) The difference in speeds of operation of the processor and memory
c) To reduce the memory access and cycle time
d) All of the mentioned

(xii) Relate: The collection of the entities where data is stored is called _____

a) Block
b) Set
c) Word
d) Byte

(xiii) Choose the correct one: Parallel processing has single execution flow.

a) 0
b) 1
c) 1
d) flase

(xiv) Choose the correct one: A term for simultaneous access to a resource, physical or logical.

a) Multiprogramming
b) Multitasking
c) Threads
d) Concurrency

(xv) Choose the correct one: _____ leads to concurrency.

a) Serialization
b) Parallelism
c) Serial processing
d) Distribution

Group-B

(Short Answer Type Questions) 3 x 5=15

2. Explain, How does a cache memory improve the performance of a computer system? (3)
3. Explain, How does a TLB work in virtual memory? (3)
4. Implement a cache memory in a computer system. (3)
5. Compare and contrast synchronous and asynchronous DRAM. (3)
6. Design a simple CPU with a control unit, ALU, and memory unit. (3)

OR

Design a memory controller for a computer system. (3)

Group-C

(Long Answer Type Questions) 5 x 6=30

7. Describe the difference between von Neumann and Harvard architectures? (5)
8. State the function of the control unit in a CPU? (5)
9. State the purpose of a memory hierarchy in computer systems? (5)
10. Tell the role of an I/O controller in a computer system? (5)
11. Evaluate the performance of a computer system with and without a TLB. (5)
12. Design a new cache coherence protocol for a multiprocessor system. (5)

OR

Design a new virtual memory algorithm for a computer system. (5)

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