

BRAINWARE UNIVERSITY

Term End Examination 2021 - 22 Programme – Bachelor of Computer Applications Course Name – Computer Organization and Architecture Course Code - BCAC202 (Semester II)

Time allotted: 1 Hrs.15 Min. Full Marks: 60 [The figure in the margin indicates full marks.] Group-A (Multiple Choice Type Question) $1 \times 60 = 60$ Choose the correct alternative from the following: (1) The ability to temporarily halt the CPU and use this time to send information on buses is called a) Direct memory access b) Vectoring the interrupt c) System Interrupt d) Cycle stealing (2) addressing mode used in the instruction PUSH B is a) Direct b) Register d) Index c) Register indirect (3) The unit of a computer system which executes program, communicates with and often controls the operation of other subsystems of the computer is the a) CPU b) Control unit c) both CPU & Control unit d) Peripheral unit (4) The addressing mode used in the instruction MOV A,B is a) Direct b) Register c) Register indirect d) Index (5) In the case of, Zero-address instruction method the operands are stored in a) Registers b) Accumulators c) Push down stack d) Cache (6) In a computer, ALU can perform a) addition b) subtraction d) all of these c) multiplication (7) When we subtract -3 from 2, the answer in 2's complement form is ... a) 0001 b) 1101 c) 0101 d) 1001

(8) 1's complement representation of decimal number of -17 by using 8 bit representation

is

a) 1110 1110	b) 1101 1101
c) 1100 1100	d) 0001 0001
(9) The 2's complement of the number 1101110 is	
a) 0010001	b) 0110001
c) 0010010	d) None of these
(10) How can you represent a decimal point?	
a) By weight decided by its position	b) By a series of coefficients
c) By location as well as base	d) None of these
(11) Which sign bit is used for representing the posi representation?	tive sign in floating point
a) 0	b) 1
c) either 1 or 0	d) None of these
(12) Which method/methods of representation of numerory than others?	imbers occupies a larger amount of
a) Sign-magnitude	b) 1's complement
c) 2's complement	d) 1's & 2's complement
(13) The advantage of I/O mapped devices to memor	ory mapped is
a) The former offers faster transfer of data	b) The devices connected using I/O mapping have a bigger buffer space
c) The devices have to deal with fewer address lines	d) No advantage as such
(14) The principle of locality justifies the use of	
a) Interrupt	b) DMA
c) Polling	d) Cache memory
(15) Micro Instruction are kept in	
a) Main memory	b) Control memory
c) Cache memory	d) Auxiliary memory
(16) The effectiveness of the cache memory is based	d on the property of
a) Locality of reference	b) Memory localization
c) Memory size	d) None of the mentioned
(17) The memory blocks are mapped on to the cache	e with the help of
a) Hash functions	b) Vectors
c) Mapping functions	d) None of the mentioned
(18) The smallest entity of memory is called	_
a) Cell	b) Block
c) Instance	d) Unit
(19) A pipeline is like-	
a) an automobile assembly line	b) house pipeline
c) Bothan automobile assembly line & house pipeline	d) a gas line
(20) Instruction pipelining has minimum sta	ges
a) 4	b) 2
c) 3	d) 6
(21) The transfer of large chunks of data with the in	volvement of the processor is done by-
a) DMA controller	b) Arbitrator
c) User system programs	d) None of the mentioned

(22) The control unit of computer	
a) Performs ALU operations on the data	b) Controls the operation of the output devices
c) both Performs ALU operations on the data & Controls the operation of the output devices	d) Directs the other unit of computers
(23) The unit which decodes and translates each instread enable signals for ALU and other units is called	ruction and generates the necessary
a) ALU	b) Control Unit
c) CPU	d) Logical Unit
(24) RISC stands for-	
a) Risk Instruction Source Computer	b) Reduced Instruction Set Computer
c) Risk Instruction Set Computer	d) Risk Instruction Set Computing
(25) The maximum performance measurement, attain	nable by the implementation is
a) Ideal pipeline CPI	b) Ideal pipeline CDI
c) Ideal pipeline CDA	d) Initial pipeline CPI
(26) Pipelining increases CPU instruction, by-	
a) Size	b) Throughput
c) Cycle rate	d) Time
(27) The contention for the usage of a hardware device	ce is called
a) Structural hazard	b) Stalk
c) Deadlock	d) None of the mentioned
(28) To put the microprocessor in the wait state	
a) lower the HOLD input	b) lower the READY input
c) raise the HOLD input	d) None of these
(29) In a microprocessor system with memory mappe	ed I/O
a) Devices have 8-bit addresses	b) Devices are accessed using IN and OUT instructions
c) There can be a maximum of 256 input devices and 256 output devices	d) Arithmetic and logic operations can be directly performed with the I/O data.
(30) In a microprocessor system, the RST instruction	will cause an interrupt
 a) only if an interrupt service routine is being executed 	b) only if a bit in the interrupt mask is made 0
 c) only if interrupts have been enabled by an EI instruction 	d) none of these
(31) In a generic microprocessor instruction cycle tin	ne is
a) Charton than machine avalating	
a) Shorter than machine cycle time	b) Larger than machine cycle time
c) Ten times the machine cycle time	
•	b) Larger than machine cycle time
c) Ten times the machine cycle time (32) Micro program is a) The name of source program in micro	b) Larger than machine cycle timed) Exactly the same as the machine cycle timeb) The set of instructions indicating the
c) Ten times the machine cycle time (32) Micro program is	b) Larger than machine cycle time d) Exactly the same as the machine cycle time
 c) Ten times the machine cycle time (32) Micro program is a) The name of source program in micro computers c) Primitive form of macros used in assembly 	b) Larger than machine cycle timed) Exactly the same as the machine cycle timeb) The set of instructions indicating the primitive operations in a system
 c) Ten times the machine cycle time (32) Micro program is a) The name of source program in micro computers c) Primitive form of macros used in assembly language programming 	b) Larger than machine cycle timed) Exactly the same as the machine cycle timeb) The set of instructions indicating the primitive operations in a system
 c) Ten times the machine cycle time (32) Micro program is a) The name of source program in micro computers c) Primitive form of macros used in assembly language programming (33) In the absolute addressing mode 	 b) Larger than machine cycle time d) Exactly the same as the machine cycle time b) The set of instructions indicating the primitive operations in a system d) Program of very small size b) Address of the operand is outside the

address is called	
a) Instruction execution	b) Straight line sequencing
c) Instruction fetch	d) Instruction Cycle
(35) Instruction cycle is	
a) fetch-decode-execution	b) fetch-execution-decode
c) decode-fetch-execution	d) None of these.
(36) A source program is usually in	
a) Assembly language	b) Machine level language
c) High-level language	d) Natural language
(37) The addressing mode used in an instruction of t	he form SUB X, Y is
a) absolute	b) immediate
c) indirect	d) relative
(38) A stack is a	
a) 32-bit register in the microprocessor	b) 16-bit register in the microprocessor
c) set of memory locations in R/W memory reserved for storing information temporarily during the execution of a program	d) 16-bit memory address stored in the h program counter
(39) Operation is normally specified in one field, known	own as
a) Operand	b) Opcode
c) Operation	d) Instruction count
(40) The instruction -> Add LOCA, R0 does	_
a) Adds the value of LOCA to R0 and stores in the temp register	b) Adds the value of R0 to the address of LOCA
c) Adds the values of both LOCA and R0 and stores it in R0	d) Adds the value of LOCA with a value in accumulator and stores it in R0
(41) In computer, ALU has	
a) 2 units	b) 3 units
c) 4 units	d) 5 units
(42) The processor keeps track of the results of its op-	perations using a flag called
a) Conditional code flags	b) Test output flags
c) Type flags	d) None of the above
(43) The Flag 'V' is set to 1 indicates that,	
a) The operation is valid	b) The operation is validated
c) The operation as resulted in an overflow	d) Both a and c
(44) -8 is equal to signed binary number?	
a) 10001000	b) 1000
c) 10000000	d) 11000000
(45) When signed numbers are used in binary arithm notations would have a unique representation for	
a) Sign-magnitude	b) 1's complement
c) 2's complement	d) 9's complement
(46) Divide overflow is generated when	
a) Sign of the dividend is different from the divisor.	b) Sign of the dividend is the same as that of the divisor.
c) The first part of the dividend is smaller than the divisor.	d) The first part of the dividend is greater than the divisor.

(4/) A floating point number that has a 0 in the MS	SB of manussa is said to have
a) Overflow	b) Underflow
c) Important number	d) Undefined
(48) In subtraction of binary numbers, if the subtrathen borrow from a significant binary significant	
a) Lower	b) Higher
c) First	d) None of the above
(49) Subtractor can be implemented using	
a) adder	b) Complementer
c) Both	d) None of these
(50) When we perform subtraction on -7 and 1 the	answer in 2's complement form is
a) 1010	b) 1110
c) 110	d) 1000
(51) The ALU makes use of to store the i	ntermediate results.
a) Accumulators	b) Registers
c) Heap	d) Stack
(52) In memory-mapped I/O	
a) The I/O devices and the memory share the same address space	b) The I/O devices have a separate address space
 c) The memory and I/O devices have an associated address space 	d) A part of the memory is specifically set aside for the I/O operation
(53) Process that periodically checks status of an I/	O devices, is known as
a) Cold swapping	b) I/O instructions
c) Polling	d) Dealing
(54) An instruction code must specify the address of	of the-
a) Operand	b) Opcode
c) Both of above	d) None of above
(55) If the CPU and I/O interface share a common units is known as?	bus than transfer of data between two
a) Asynchronous	b) Clock dependent
c) Synchronous	d) Decoder independent
(56) Which table handles store address of interrupt	handling subroutine?
a) Vector table	b) Symbol link table
c) Interrupt vector table	d) None of above
(57) How many RAM chips of size (256 X 1bit) ar Memory?	re required to build (1024 X 1bit)
a) 24	b) 4
c) 32	d) 8
(58) The bit used to signify that the cache location	is updated is
a) Dirty bit	b) Update bit
c) Reference bit	d) Flag bit
(59) In associative mapping, in a 16 bit system the	, •
a) 12	b) 8
c) 9	d) 10
(60) The collection of the entities where data is sto	,

a) Block

c) Word

b) Set

d) Byte