BRAINWARE UNIVERSITY

Term End Examination 2021 - 22
Programme – Diploma in Computer Science & Engineering
Course Name – Microprocessors
Course Code - DCSE404
(Semester IV)

Time allotted : 1 Hrs.15 Min. **Full Marks : 60**

[The figure in the margin indicates full marks.]

Group-A

(Multiple Choice Type Question) 1 x 60=60

Choose the correct alternative from the following :

(1) Why 8085 Processor is called an 8-bit processor?

a) Because 8085 processor has 8-Bit ALU
b) Because 8085 processor has 8-Bit data bus
c) Both (Because 8085 processor has 8-Bit ALU) and (Because 8085 processor has 8-Bit data bus)
d) None of these

(2) Which of the following is a user programmable register?

a) Memory Address Register
b) General purpose register Register
c) Flag register
d) Program Counter

(3) HLT is a _____ instruction

a) 1 Byte
b) 2 Byte
c) 3 Byte
d) 4 Byte

(4) In a computer where microprocessor is used as CPU is known as

a) Microprocessor
b) Micro-computer
c) Microcontroller
d) All of these

(5) Which flag is used for BCD Addition?

a) Carry
b) Auxiliary Carry
c) Parity
d) Sign

(6) Which one requires 4 t-States to complete?

a) Memory Read
b) I/O Write
c) Op-code Fetch
d) Memory Write

(7) Which stack is used in 8085?

a) FIFO
b) LIFO
c) FILO
d) None of these

(8) What are the Control signals used for DMA operation?

a) INT and INTA
b) IN and OUT
c) HOLD and HLDA
d) None of these

(9) What is meant by Maskable interrupts?

a) An Interrupt which can never be Turned off
b) An Interrupt that can be turned off by the programmer
c) Both (An Interrupt which can never be Turned off) and (An Interrupt that can be turned off by the programmer)
d) None of these

(10) Vector Address of RST 3 is

a) 0020H
b) 0018H
c) 0081H
d) None of these

(11) Which one has the highest priority

a) TRAP
b) RST 7.5
c) INTR
d) HOLD

(12) Addressing mode of MOV A, B is

a) Register Direct
b) Memory Direct
c) Memory Indirect
d) Base Register

(13) In a 3-Byte instruction, first byte always stores

a) Lower order Address
b) Higher order address
c) Op-code
d) Operand

(14) After XRA A, content of A will be always

a) 0
b) 1
c) 2
d) 3

(15) Which flag is associated with JZ 8050H instruction?

a) Auxiliary Carry
b) Carry
c) Zero
d) Sign

(16) What is the addressing mode of PUSH B instruction?

a) Immediate
b) Implied
c) Register Direct
d) Stack

(17) Length of the instruction POP D is

a) 1 Byte
b) 2 Byte
c) 3 Byte
d) 4 Byte

(18) Which general register or general register pair is incremented / decremented by 2 during PUSH and POP instructions?

a) HL
b) DE
c) Stack Pointer
d) Program Counter

(19) Maximum numbers of addresses supported by peripheral-mapped-I/O is

a) 128
b) 256
c) 512
d) 1024

(20) What is SIM?

a) Select Interrupt Mask
b) Sorting Interrupt Mask
c) Set Interrupt Mask
d) None of these

(21) How many address lines in a 2048 x 8 EPROM CHIP?

a) 10 Address Lines
b) 11 Address Lines
c) 14 Address Lines
d) 15 Address Lines

(22) Third state of a tri-state device is

a) High
b) Low
c) High-Impedance
d) Both High and Low

(23) Data bus width of Intel 8086 is

a) 10 bit
b) 8 bit
c) 16 bit
d) 20 bit

(24) The _____ is used to connect more microprocessor

a) Peripheral
b) Cascade
c) I/O devices
d) Control unit

(25) The index register is used to hold

a) Memory Register
b) Offset Register
c) Segmented Memory
d) Offset Memory

(26) To interface a memory with 1024 locations, how many address lines will be used?

a) 10
b) 11
c) 12
d) 16

(27) Why 8085 Processor is called an 8-bit processor?

a) Because 8085 processor has 8-Bit ALU.
b) Because 8085 processor has 8-Bit data bus.
c) Because 8085 processor has 8-Bit control bus.
d) None of these

(28) Which of the following is a user programmable register?

a) Memory Address Register
b) Data Register
c) Program Counter
d) Accumulator

(29) Maximum numbers of memory location supported by 8085?

a) 10000
b) 32768
c) 65536
d) No limit

(30) JNZ is one kind of _____ operation

a) Data transfer
b) Arithmetic
c) Branching
d) Machine Control

(31) Which is a 16 bit register?

a) Accumulator
b) Flag
c) Program Counter
d) Register C

(32) How many general Purpose registers are present in 8085?

a) 3
b) 4
c) 5
d) 6

(33) LDA 8050H requires ____ numbers of machine cycle

a) 3
b) 1
c) 4
d) None of This

(34) Which one is closely related with Clock pulse?

a) Instruction Cycle
b) Machine Cycle
c) T-States
d) None of these

(35) MOV A, B requires how many machine cycles?

a) 1
b) 2
c) 3
d) 4

(36) Which of the following is hardware interrupts?

a) RST5.5, RST6.5, RST7.5
b) INTR, TRAP
c) Both (a) and (b)
d) None of This

(37) The Maskable interrupt is

a) An Interrupt which can never be Turned off
b) An Interrupt that can be turned off by the programmer
c) Both (a) and (b)
d) None of these

(38) Address line for RST0 is?

a) 0020H
b) 0028H
c) 0000H
d) 0038H

(39) Which one has even higher priority than TRAP?

a) RST 7.5
b) RST 5.5
c) HOLD
d) None of these

(40) In DAD instruction, one of the operands always stored in _____ register pair

a) PSW
b) BC
c) DE
d) HL

(41) LDA 8050H is a

a) 1 –Byte Instruction
b) 2 –Byte Instruction
c) 3 –Byte Instruction
d) 4 –Byte Instruction

(42) When DMA controller works as a normal peripheral device, it acts in

a) Master Mode
b) Slave Mode
c) Both (a) and (b)
d) None of This

(43) An interrupt that can be turned off by the programmer is known as

a) Maskable Interrupt
b) Non-Maskable Interrupt
c) Software Interrupt
d) Priority Interrupt

(44) For MOV A, M instruction, one of the operand will be stored in

a) HL
b) Accumulator
c) Address of operand will be stored in HL
d) None of these

(45) Which statement is true for NOP instruction?

a) 1 –Byte Instruction
b) 2 –Byte Instruction
c) 3 –Byte Instruction
d) 4 –Byte Instruction

(46) Addressing mode of MOV B, C instruction is

a) Immediate
b) Implied
c) Register Direct
d) Stack

(47) In a subroutine program, last instruction is always a _____ instruction

a) Conditional jump
b) Unconditional jump
c) Return
d) None of these

(48) Deleting an entry from a stack memory can be done by _____ instruction

a) PUSH
b) MOV
c) POP
d) LDA

(49) HLT op-code means

a) Load data to accumulator
b) Store result in memory
c) Load accumulator with content of register
d) End of program

(50) In Intel 8085A microprocessor ALE signal is made high to

a) Enable the data bus to be used as low order address bus
b) To latch data D0-D7 from data bus
c) To disable data bus
d) To achieve all the functions listed above

(51) Assertion(A): Address bus is unidirectional. Reason(R): Data bus is bidirectional

a) Both A & R are true and R is the correct explanation of A
b) Both A & R are true but R is not the correct explanation of A
c) A is true but R is false
d) A is false but R is true

(52) RST0 - RST7 are the _____ in 8085.

a) hardware interrupts
b) logical interrupts
c) software interrupts
d) conditional interrupts

(53) An 8K*8 ROM, holding the monitor program in a microprocessor trainer kit has end address

a) 3FFF H
b) 2FFF H
c) 1FFF H
d) None of these

(54) If 300 peripheral device need to be interfaced with 8085, which should be preferred?

a) Memory-mapped I/O
b) Peripheral-mapped I/O
c) Any one
d) None of these

(55) If 1000 peripheral device need to be interfaced with 8085, which should be preferred?

a) Memory-mapped I/O
b) Memory-mapped I/O
c) Any one
d) None of these

(56) In Memory-mapped-I/O, every device address is of

a) 8 bit
b) 16 bit
c) 24 bit
d) 32 bit

(57) 8005H location can be used as a peripheral address in which method?

a) Memory-mapped I/O
b) Peripheral -mapped I/O
c) Any one
d) None of these

(58) An 16K*8 ROM, holding the monitor program in a microprocessor trainer kit has end address

a) 1FFF H
b) 2FFF H
c) 3FFF H
d) 4FFF H

(59) Address bus width of Intel 8086 is

a) 10 bit
b) 8 bit
c) 16 bit
d) 20 bit

(60) The RD, WR, M/IO are the heart of control for _____ mode

a) Minimum
b) Maximum
c) Halt
d) Fetch