BRAINWARE UNIVERSITY

Term End Examination 2021 - 22
Programme – Bachelor of Technology in Computer Science & Engineering
Course Name – Computer Organization and Architecture
Course Code - PCC-CS401
(Semester IV)

Time allotted : 1 Hrs.15 Min. **Full Marks : 60**

[The figure in the margin indicates full marks.]

Group-A

(Multiple Choice Type Question) 1 x 60=60

Choose the correct alternative from the following :

(1) Boolean algebra is also known as
  a) Counting algebra b) Switching algebra
  c) Transistor algebra d) Gate algebra

(2) The addressing mode, where the operand value is directly specified is
  a) implied b) direct
  c) immediate d) indirect

(3) Which of the following is not a bus?
  a) control bus b) data bus
  c) program bus d) address bus

(4) Which of the following is used to store the address of next instruction?
  a) Accumulator b) MAR
  c) Program Counter d) MDR

(5) In half subtractor, the difference circuit is implemented using …..… gate.
  a) XOR b) NOR
  c) OR d) XNOR

(6) Which of the architecture is power efficient?
  a) ISA b) RISC
  c) IANA d) CISC

(7) To reduce the memory access time we generally make use of _____
  a) SDRAM's b) Heaps
  c) Cache's d) Higher capacity RAM's

(8) The instructions like MOV or ADD are called as

a) OP-Code
b) Commands
c) Operators
d) None of above

(9) In which addressing mode the address of the operand is specified?

a) Absolute
b) Immediate
c) Indirect
d) Direct

(10) MRI indicates

a) Memory Reference Information
b) Memory Reference Instruction
c) Memory Registers Instruction
d) Memory Register information

(11) Memory management technique where allocated size is fixed -

a) paging
b) segmentation
c) fragmentation
d) indexing

(12) Associative memory is …… than RAM.

a) faster
b) same
c) slower
d) does not depend

(13) Memory management technique where allocated size varies-

a) paging
b) segmentation
c) fragmentation
d) indexing

(14) If the required page is not present in the main memory, it is said to be

a) Page hit
b) Page fault
c) Page miss
d) Page skip

(15) Which of the following mapping technique does not use any type of mapping function?

a) Direct
b) Associative
c) Non-direct
d) Set associative

(16) If size of cache memory is 1K and one block contains 8 words of 2 bytes each, what is the number of cache blocks?

a) 64
b) 65
c) 33
d) 32

(17) If 'h' is the hit then (1-h) is

a) hit ratio
b) miss
c) miss ratio
d) hit rate

(18) Registers are ……. speed storage devices.

a) low
b) high
c) medium
d) None of these

(19) Which address belongs to RAM?

a) physical address
b) absolute address
c) logical address
d) relative address

(20) Which operation/s is/are responsible for data hazards?

a) read
b) write
c) Both of these
d) None of these

(21) A register used to hold the instruction being executed is

a) IR
b) MAR

c) AC
d) MDR

(22) Data consistency is related with …….
a) Locality
b) Coherence
c) Inclusion
d) Capability

(23) Which of the following stores the information only till power supply?
a) SRAM
b) RAM
c) DRAM
d) Cache

(24) Which is/are register?
a) PC
b) MAR
c) AC
d) All of these

(25) The ratio of hit to the total number of memory references is called
a) hit ratio
b) miss ratio
c) miss rate
d) hit rate

(26) The property where nearby data are accessed?
a) temporal
b) parallel
c) spatial
d) sequential

(27) Run time mapping from virtual to physical address is done by
a) Memory management unit
b) CPU
c) PC
d) None of these

(28) Cache memory acts between
a) CPU and RAM
b) CPU and registers
c) RAM and ROM
d) None of these

(29) Which of the following has smallest capacity
a) cache memory
b) RAM
c) secondary memory
d) registers

(30) How many address lines are needed to address each memory locations in a 2048 x 4 memory chip?
a) 10
b) 11
c) 8
d) 12

(31) A register capable of shifting its binary information either to the right or the left is called a
a) parallel register
b) serial register
c) shift register
d) storage register

(32) The average time required to reach a storage location in memory and obtain its contents is called
a) Latency time
b) Access time
c) Turnaround time
d) Response time

(33) A memory used to store frequent used data
a) stack pointer
b) accumulator
c) cache
d) disk buffer

(34) The memory unit that communicates directly with the CPU is called the
a) main memory
b) Secondary memory
c) shared memory
d) auxiliary memory

(35) The algorithm to remove and place new contents into the cache is called

a) Renewal algorithm
b) Replacement algorithm
c) Mapping algorithm
d) None of these

(36) Which of the following is not a property of memory module?

a) Locality
b) Coherence
c) Inclusion
d) Capability

(37) The pipelining process is also called as ……

a) Superscalar operation
b) Assembly line operation
c) Von Neumann cycle
d) None of the mentioned

(38) The fetch and execution cycles are interleaved with the help of

a) Modification in processor architecture
b) Clock
c) Special unit
d) Control unit

(39) …… is used to represent segment utilization as a function of time in pipelining.

a) Block diagram
b) Time diagram
c) Space time diagram
d) Space diagram

(40) Total number of clock cycles in pipelining is given by……. (where n = number of instruction and k = number of stages)

a) k-n-1
b) k+n-1
c) k-n+1
d) k+n+1

(41) Overlapping of stages is a concept of

a) pipelining
b) sequential processing
c) parallel processing
d) All of these

(42) The ratio of time of execution in non pipelined architecture to the time of execution in pipelined architecture is known as

a) Speedup
b) Efficiency
c) Throughput
d) Execution time

(43) The mapping technique which stores three words with different tag but with same index is

a) 2 way set associative
b) 1 way set associative
c) 3 way set associative
d) 4 way set associative

(44) Which mapping technique cannot store more than one data with same index?

a) Direct
b) Set associative
c) Associative
d) All of these

(45) MISD stands for

a) Multiple instruction single data
b) Memory instruction single data
c) Multiple instruction sequence data
d) Multiple information single data

(46) Uniprocessor is related to which of the following classification?

a) SIMD
b) SISD
c) MISD
d) MIMD

(47) Multiprocessor is related to which of the following classification?

a) SIMD
b) SISD
c) MISD
d) MIMD

(48) Which is/are data hazard

a) WAR
b) RAW
c) WAW
d) All of above

(49) SISD stands for

a) Single instruction single data
b) Single information single data
c) Sequence instruction single data
d) Single instruction sequence data

(50) In which cycle the memory is read and the contents of memory at the address contained in the PC register are loaded into Instruction Register

a) Execution Cycle
b) Memory Cycle
c) Decode Cycle
d) Fetch Cycle

(51) The step during which the operations specified by the instruction are processed

a) Decode
b) Fetch
c) Execute
d) none of these

(52) Which of the following is not a data hazard?

a) WAR
b) RAW
c) RAR
d) WAW

(53) Each stage in pipelining generally completed within …….. cycle.

a) 1
b) 2
c) 3
d) 4

(54) In DMA, the value of ……. register is incremented after each word transfer.

a) Control register
b) Address register
c) Word count register
d) Buffer register

(55) Register which specifies the mode of transfer in DMA is

a) Control register
b) Address register
c) Word count register
d) Buffer register

(56) DMA controller transfer data without intervention of

a) MU
b) CPU
c) ALU
d) PC

(57) An interface that provides a method for transferring binary information between internal storage and external devices is called

a) I/O interface
b) Input interface
c) Output interface
d) I/O bus

(58) The device which is used to connect a peripheral to a bus is called

a) Control Register
b) Interface
c) Communication Protocol
d) None of these

(59) Interrupt initiated by instructions is called

a) Software interrupt
b) External interrupt
c) Hardware interrupt
d) All of these

(60) ……. is used to choose between incrementing the PC or performing ALU operations.

a) Conditional codes
b) Multiplexer
c) Control unit
d) None of these