

## **BRAINWARE UNIVERSITY**

## Term End Examination 2021 - 22

## Programme – Bachelor of Technology in Electronics & Communication Engineering Course Name – Microcontrollers Course Code - PCC-EC403 (Semester IV)

Time allotted: 1 Hrs.15 Min. Full Marks: 60

[The figure in the margin indicates full marks.]

## Group-A

(Multiple Choice Type Question)

1 x 60=60

Choose the correct alternative from the following:

(1) Consider the following registers: 1. Accur	mulator and flag register 2. B and C register 3. D
and E register 4. H and L register Which	of these 8-bit registers of 8085 microprocessor
can be paired together to make a 16-bit re	gister?

a) 1,3 and 4

b) 2,3 and 4

c) 1,2 and 4

d) 1,2 and 3

- (2) ALU (Arithmetic and Logic Unit ) of 8085 microprocessor consists of
  - a) Accumulator, temporary register, arithmetic and logic circuits
  - c) Accumulator, arithmetic and logic circuits
- b) Accumulator, arithmetic, logic circuits and five flags
- d) Accumulator, temporary register, arithmetic, logic circuits and five flags
- (3) Which of the following microprocessors is a 4 bit microprocessor?

a) 4004

b) 8080

c) 8085

d) Z80

- (4) The program counter in a 8085 micro-processor is a 16-bit register, because
  - a) It counts 16-bits at a time

b) There are 16 address lines

c) It facilitates the user storing 16-bit data temporarily

- d) It has to fetch two 8-bit data at a time
- (5) In an intel 8085A microprocessor, why is READY signal used?
  - a) To indicate to user that the microprocessor is working and is ready for use
- b) To provide proper WAIT states when the microprocessor is communicating with a slow peripheral device
- c) To slow down a fast peripheral device so as to communicate at the microprocessor's device
- (a) None of these

(6) Which semiconductor technology is used for fa	abrication of 8085 microprocessor?
a) ECL	b) NMOS
c) NMOS and HMOS	d) NMOS and CMOS
(7) The frequency of the driving network connected microprocessor is	ed between pins 1 and 2 of 8085
a) twice the desired frequency	b) equal to the desired frequency
c) four times the desired frequency	d) none of these
(8) A microprocessor is a	
a) SSI device	b) MSI device
c) LSI device	d) VLSI device
(9) Accumulator based microprocessor example a	re:
a) Intel 8085	b) Motorola 6809
c) Intel 8085 and Motorola 6809	d) None of these
(10) The address / data bus in 8085 is	
a) multiplexed	b) demultiplexed
c) decoded	d) encoded
(11) What is the meaning of the instruction MVI A	,05H?
a) data 05H is stored in the accumulator	b) fifth bit of accumulator is set to one
c) address 05H is stored in the accumulator	d) none of the mentioned
(12) Which one of the following is called non-vector	ored interrupt?
a) TRAP	b) INTR
c) RST 7.5	d) RST 0
(13) In 8085 microprocessor, the RST6 instruction location	transfer Programme execution to following
a) 0030H	b) 0032H
c) 0048H	d) 0024H
(14) Which interrupt has the highest priority?	
a) INTR	b) TRAP
c) RST6.5	d) RST6.6
(15) Which interrupt is not level sensitive in 8085?	
a) RST 6.5	b) RST 7.5
c) RST 5.5	d) RST 4.5
(16) By issuing which one of the following signal, controller?	CPU releases the system bus to DMA
a) HOLD	b) HLDA
c) ALE	d) READY
(17) In 8086 microprocessor the following has the l	highest priority among all type interrupts?
a) NMI	b) DIV 0
c) TYPE 255	d) OVER FLOW
(18) In 8086 microprocessor one of the following s	tatements is not true?
a) coprocessor is interfaced in max mode	b) coprocessor is interfaced in min mode
c) i/o can be interfaced in max / min mode	d) supports pipelining

(19) 8088 microprocessor differs with 8086 micropro	cessor in
a) data width on the output	b) address capability
c) support of coprocessor	d) support of MAX / MIN mode
(20) Which of the following is a four byte instruction	?
a) MOV AX, 2345	b) MUL BX
c) DIV CL	d) ADD AX, [BP+0200]
(21) 16 bit register of 8086 consist of	
a) 16 flags	b) 8 flags
c) 9 flags	d) 7 flags
(22) Which of the following instruction is a logical in	astruction?
a) DIV AB	b) TEST
c) CALL	d) AAM
(23) DS Stand for	
a) Data segment	b) Direct segment
c) Declare segment	d) Divide segment
(24) Which of the following registers are not bit addre	essable?
a) SCON	b) PCON
c) A	d) PSW
(25) A microcontroller at-least should consist of	
<ul> <li>a) RAM, ROM, I/O devices, serial and parallel ports and timers</li> </ul>	b) CPU, RAM, I/O devices, serial and parallel ports and timers
<ul> <li>c) CPU, RAM, ROM, I/O devices, serial and parallel ports and timers</li> </ul>	d) CPU, ROM, I/O devices and timers
(26) LCALL instruction takes	
a) 2 bytes	b) 4 bytes
c) 3 bytes	d) 1 byte
(27) The first microprocessor was	
a) 4001	b) 4002
c) 4003	d) 4004
(28) The microprocessor was introduced in the year	
a) 1940	b) 1971
c) 1973	d) 1980
(29) The number of output pins in 8085 microprocess	sors are
a) 27	b) 40
c) 19	d) 28
(30) Which pin is used for demultiplexing of address	and data bus of 8085 microprocessor?
a) TRAP	b) ALE
c) IO/M′	d) READY
(31) In 8085 microprocessor, name the 16 bit register	is called
a) Stack Pointer	b) PSW
c) Both Stack Pointer and PSW	d) None of these
(32) Intel 8085A microprocessor ALE signal is made	high to

<ul> <li>a) Enable the data bus to be used as low order address bus</li> </ul>	b) To latch data D0-D7 from data bus
c) To disable data bus	d) To achieve all the functions listed above
(33) Consider the following statements: In 8085 micromultiplexed in order to I)Increase the speed of m pins. III)Connect more peripheral chips. Which of	icroprocessor. II)Reduce the number of
a) (I) only	b) (I) Only
c) (II) & (III)	d) (I), (III) & (IV)
(34) If the microprocessor is capable of addressing 64 is	Kbytes of memory, its address bus width
a) 16 bits	b) 20 bits
c) 8 bits	d) none of these
(35) In 8085 name of the 16 bit registers is	
a) stack pointer	b) program counter
c) Stack pointer and program counter	d) none of these
(36) Temporary registers in 8085 are	
a) B and C	b) D and E
c) H and L	d) W and Z
(37) The word size of 8085 microprocessor is	
a) 8-bits	b) 16-bits
c) 20-bits	d) 4-bits
(38) How many times will the following loop be exec DCRC JNZ LOOP	euted? XRA A MVI C, 05H LOOP;
a) once	b) five
c) infinite times	d) four times
(39) The address bus of microprocessor is	
a) unidirectional	b) bi-directional
c) unidirectional as well as bi-directional	d) none of these
(40) The parity flag of 8085 microprocessor is set to I	HIGH when
a) The total number of 1's is odd	b) The total number of 1's is even
c) The total number of 1's is odd and the total number of 1's is even	d) None of these
(41) What does microprocessor speed depends on?	
a) Clock	b) Data bus width
c) Address bus width	d) Control bus width
(42) After execution of instruction RRC, which one o	f the following flag will be affected
a) Auxiliary Flag	b) Zero Flag
c) Sign Flag	d) Carry Flag
(43) The CALL location for TRAP is	
a) 0023H	b) 0032H
c) 0042H	d) 0024H
(44) The number of T-States required for PCHL instru	action execution is
a) 4	b) 6

c) 8	d) 10
(45) Let 81H & C2H are added. The RAR is executed.	The content of the Accumulator will be
a) 82H	b) 87H
c) 90H	d) 97H
(46) HLT op-code means	
a) Load data to accumulator.	b) Store result in memory.
c) Load accumulator with contents of register.	d) End of program
(47) XCHG is an	
a) data transfer instruction	b) logical instruction
c) arithmatic instruction	d) none of these
(48) In an Intel 8085A, which is the first machine cycle	e of an instruction?
a) An op-code fetch cycle	b) A memory write cycle
c) A memory read cycle	d) An I/O read cycle
(49) Which of the following instruction is not possible	in 8085?
a) POP PSW	b) POP B
c) POP D	d) POP 30 H
(50) Which instruction is required to rotate the content carry?	of accumulator one bit right along with
a) RLC	b) RAL
c) RRC	d) RAR
(51) What is the RST for the TRAP?	
a) RST5.5	b) RST4.5
c) RST4	d) RST3
(52) What are software interrupts?	
a) RST 0-7	b) RST 5.5 - 7.5
c) INTR, TRAP	d) RST 4.4 - 6.4
(53) STA 2070H is an instruction of	
a) One byte	b) two byte
c) three byte	d) four byte
(54) STA 3526H is an instruction of	
a) direct addressing mode	b) indirect addressing mode
c) register addressing mode	d) Immediate addressing mode
(55) CMA is an instruction of	
a) direct addressing mode	b) indirect addressing mode
c) register addressing mode	d) Implicit addressing mode
(56) During IO operation the IO/M ' signal will be	
a) LOW	b) Tristate
c) HIGH	d) None of these
(57) In 8086 microprocessor, the size of each segment is	
a) 32 KB	b) 64 KB
c) 16 KB	d) 8 KB
(58) In which year 8086 microprocessor was introduce	A?

a) 1978
c) 1977
d) 1971
(59) In which year, 8088 microprocessor was announced?
a) 1979
b) 1988
c) 1999
d) 2000
(60) 8088 microprocessor has
a) 16 bit data bus
b) 4 byte pre-fetch queue
c) 6 byte pre-fetch queue
d) 16 bit address bus