BRAINWARE UNIVERSITY

Term End Examination 2021 - 22
Programme – Bachelor of Computer Applications
Course Name – Microprocessor and Microcontroller
Course Code - BCA403
(Semester IV)

Time allotted : 1 Hrs.25 Min. **Full Marks : 70**

[The figure in the margin indicates full marks.]

Group-A

(Multiple Choice Type Question) 1 x 70=70

Choose the correct alternative from the following :

(1) Why 8085 processor is called an 8 bit processor?
a) because 8085 processor has 8 bit ALU
b) because 8085 processor has 8 bit data bus
c) because 8085 processor has 16 bit data bus
d) because 8085 processor has 16 bit address bus

(2) A microprocessor is a
a) SSI device
b) MSI device
c) LSI device
d) VLSI device

(3) The microprocessor was introduced in the year
a) 1940
b) 1971
c) 1973
d) 1980

(4) 8085 microprocessor has how many pins
a) 40
b) 39
c) 42
d) 20

(5) Which of the following microprocessors is a 4 bit microprocessor?
a) 4004
b) 8080
c) 8085
d) 8086

(6) In a computer where microprocessor is used as CPU is known as
a) Microprocessor
b) Micro-computer
c) Microcontroller
d) All of these

(7) Intel 8085A microprocessor ALE signal is made high to

a) Enable the data bus to be used as low order address bus
b) To latch data D0-D7 from data bus
c) To disable data bus
d) To achieve all the functions listed above

(8) An 8-bit microprocessor has an

a) 8 bit data bus
b) 8-bit address bus
c) 8-bit control bus
d) 8-bit interrupt lines

(9) In an intel 8085A microprocessor, why is READY signal used?

a) To indicate to user that the microprocessor is working and is ready for use
b) To provide proper WAIT states when the microprocessor is communicating with a slow peripheral device.
c) To slow down a fast peripheral device so as to communicate at the microprocessor's device
d) None of the above

(10) Which of the following statements for Intel 8085 is correct?

a) Program Counter (PC) specifies the address of the instruction last executed
b) PC specifies the address of the instruction being executed
c) PC specifies the address of the instruction to be executed
d) PC specifies the number of instructions executed so far

(11) In 8085 name of the 16 bit registers is

a) stack pointer
b) program counter
c) Stack pointer and program counter
d) none of these

(12) The word size of 8085 microprocessor is

a) 8-bits
b) 16-bits
c) 20-bits
d) 4-bits

(13) How many times will the following loop be executed? XRA A MVI C, 05H LOOP; DCR C JNZ LOOP

a) once
b) five
c) infinite times
d) four times

(14) The address bus of microprocessor is

a) unidirectional
b) bi-directional
c) unidirectional as well as bi-directional
d) none of these

(15) The address / data bus in 8085 is _____.

a) multiplexed
b) demultiplexed
c) decoded
d) encoded

(16) What does microprocessor speed depends on?

a) Clock
b) Data bus width
c) Address bus width
d) Control bus width

(17) In 8085 microprocessor, for execution of the instruction DCX Rp (Rp is register pair) how many T-states are required?

a) 6
b) 4
c) 3
d) 1

(18) After execution of instruction RRC, which one of the following flag will be affected

a) Auxiliary Flag
b) Zero Flag
c) Sign Flag
d) Carry Flag

(19) The CALL location for TRAP is

a) 0023H
b) 0032H
c) 0042H
d) 0024H

(20) When CALL instruction is executed, the SP will be

a) SP-1
b) SP+1
c) SP-2
d) SP+2

(21) In 8085 microprocessor, the RST6 instruction transfer Programme execution to following location

a) 0030H.
b) 0032H.
c) 0048H.
d) 0024H.

(22) XCHG is an

a) data transfer instruction
b) logical instruction
c) arithmatic instruction
d) none of these

(23) What is meant by maskable interrupts?

a) an interrupt which can never be turned off
b) an interrupt that can be turned off by the programmer
c) an interrupt which can never be turned on
d) an interrupt which can never be turned on or off

(24) How many T-states are required for execution of OUT 80H instruction?

a) 10
b) 13
c) 16
d) 7

(25) What is the RST for the TRAP?

a) RST5.5
b) RST4.5
c) RST4
d) RST3

(26) What are level Triggering interrupts?

a) INTR & TRAP
b) RST6.5 & RST5.5
c) RST7.5 & RST6.5
d) RST2.5 & RST6.2

(27) Which interrupt is not level sensitive in 8085?

a) RST 6.5
b) RST 7.5
c) RST 5.5
d) RST 4.5

(28) What are software interrupts?

a) RST 0-7
b) RST 5.5 - 7.5
c) INTR, TRAP
d) RST 4.4 - 6.4

(29) MOV A, C is an instruction of

a) One byte
b) two byte
c) three byte
d) four byte

(30) LXI H, 2500 H is an instruction of

a) direct addressing mode
b) indirect addressing mode

c) register addressing mode
d) Immediate addressing mode

(31) MVI A, 58H is an instruction of

a) direct addressing mode
b) indirect addressing mode
c) register addressing mode
d) Immediate addressing mode

(32) During IO operation the IO/M ´ signal will be

a) LOW
b) Tristate
c) HIGH
d) None of these

(33) The technique of assigning a memory address to each I/O device in the computer system i s called:

a) memory-mapped I/O
b) ported I/O
c) dedicated I/O
d) wired I/O

(34) 8086 has

a) 16 bit data bus and 20 bit address bus
b) 8 bit data bus and 20 bit address bus
c) 16 bit data bus and 16 bit address bus
d) 8 bit data bus and 16 bit address bus

(35) The Microcontroller 8051 is

a) 8-bit processor
b) 16-bit processor
c) 32-bit processor
d) 64-bit processor

(36) How many register banks are present in 8051 microcontroller?

a) 4
b) 3
c) 2
d) 1

(37) 8051 series of microcontrollers are made by which of the following companies?

a) Atmel
b) Philips
c) Atmel & Philips
d) None of the mentioned

(38) AT89C2051 has RAM of:

a) 128 bytes
b) 256 bytes
c) 64 bytes
d) 512 bytes

(39) When the microcontroller executes some arithmetic operations, then the flag bits of which register are affected?

a) PSW
b) SP
c) DPTR
d) PC

(40) Which of the following comes under the indexed addressing mode?

a) MOVX A, @DPTR
b) MOVC @A+DPTR,A
c) MOV A,R0
d) MOV @R0,A

(41) Which instruction is used to check the status of a single bit?

a) MOV A,P0
b) ADD A,#05H
c) JNB PO.0, label
d) CLR P0.05H

(42) How many bytes of bit addressable memory is present in 8051 based microcontrollers?

a) 8 bytes
b) 32 bytes
c) 16 bytes
d) 128 bytes

(43) When 8051 wakes up then 0x00 is loaded to which register?

a) DPTR
b) SP
c) PC
d) PSW

(44) A microcontroller at-least should consist of

a) RAM, ROM, I/O devices, serial and parallel p orts and timers
b) CPU, RAM, I/O devices, serial and parallel po rts and timers
c) CPU, RAM, ROM, I/O devices, serial and par allel ports and timers
d) CPU, ROM, I/O devices and timers

(45) Which of the following are 16 bit register in 8051 microcontroller?

a) DPTR
b) IE
c) TMOD
d) PC

(46) Which of the following register can be used to hold address of byte in the memory of 805 1?

a) DPTR
b) PCON
c) SBUF
d) PSW

(47) Which of the following register can be used as two individual 8 bit register in 8051?

a) DPTR
b) PC
c) SBUF
d) PSW

(48) In 8051 which interrupt has highest priority?

a) IE1
b) TF0
c) IE0
d) TF1

(49) The 8051 microcontroller is of ___pin package as a _____ processor.

a) 30, 1byte
b) 20, 1 byte
c) 40, 8 bit
d) 40, 8 byte

(50) On power up, the 8051 uses which RAM locations for register R0- R7

a) 00-2F
b) 00-07
c) 00-7F
d) 00-0F

(51) LCALL instruction takes

a) 2 bytes
b) 4 bytes
c) 3 bytes
d) 1 byte

(52) Which of the following instruction is incorrect?

a) CPL A
b) SWAP A
c) CLR C
d) RL B

(53) What is the addressing mode of MOV A, 40

a) direct addressing
b) indirect addressing
c) index addressing
d) register addressing

(54) CALL 8000H is an instruction of

a) direct addressing mode
b) indirect addressing mode
c) register addressing mode
d) Immediate addressing mode

(55) What is RIM in context of microprocessor?

a) Ready Interrupt Mask
b) Reading Interrupt Mask

c) Read Interrupt Mask
d) Read Integer Mask

(56) In 8085 microprocessor address line for RST3 is?

a) 0020H
b) 0028H
c) 0018H
d) 0019H

(57) STA 8500H is executed by

a) one machine cycle
b) two machine cycle
c) three machine cycle
d) four machine cycle

(58) MOV A,C is executed by

a) one machine cycle
b) two machine cycle
c) three machine cycle
d) four machine cycle

(59) OUT 02H is executed by

a) one machine cycle
b) two machine cycle
c) three machine cycle
d) four machine cycle

(60) A two byte instruction consists of

a) opcode and operand
b) opcode only
c) opcode and two operands
d) operand only

(61) IN 00H is an instruction of

a) direct addressing mode
b) indirect addressing mode
c) register addressing mode
d) Immediate addressing mode

(62) Which processor can address 1024KB of memory?

a) 8085
b) 8086
c) Both 8085 & 8086
d) 8088

(63) ADD B is executed by

a) one machine cycle
b) two machine cycle
c) three machine cycle
d) four machine cycle

(64) LDAX D is an instruction of

a) direct addressing mode
b) indirect addressing mode
c) register addressing mode
d) Immediate addressing mode

(65) LHLD 2500H is an instruction of

a) direct addressing mode
b) indirect addressing mode
c) register addressing mode
d) Immediate addressing mode

(66) ADD B is an instruction of

a) direct addressing mode
b) indirect addressing mode
c) register addressing mode
d) Immediate addressing mode

(67) ADI, 01 H is an instruction of

a) direct addressing mode
b) indirect addressing mode
c) register addressing mode
d) Immediate addressing mode

(68) STA 3200 H is an instruction of

a) direct addressing mode
b) indirect addressing mode

c) register addressing mode
d) Immediate addressing mode

(69) CMP B is an instruction of

a) direct addressing mode
b) indirect addressing mode
c) register addressing mode
d) Immediate addressing mode

(70) DCR C is an instruction of

a) direct addressing mode
b) indirect addressing mode
c) register addressing mode
d) Immediate addressing mode