BRAINWARE UNIVERSITY

Term End Examination 2021 - 22
Programme – Bachelor of Technology in Electronics & Communication Engineering
Course Name – VLSI Devices and Design
Course Code - PCC-EC603
(Semester VI)

Time allotted : 1 Hrs.15 Min. **Full Marks : 60**

[The figure in the margin indicates full marks.]

Group-A

(Multiple Choice Type Question) 1 x 60=60

Choose the correct alternative from the following :

(1) VLSI technology uses _____ to form integrated circuit.

a) transistors b) switches
c) diodes d) buffers

(2) Large-scale integration has _____ number of transistors.

a) 10 to 500 b) 1 to 10
c) 20,000 to 1,000,000 d) 500 to 20,000

(3) As die size shrinks, the complexity of making the photomasks _____

a) increases b) decreases
c) remains the same d) cannot be determined

(4) What is the design flow of VLSI system? i. architecture design ii. circuit design iii. logic design iv. physical design

a) ii-i-iii-iv b) iv-i-iii-ii
c) iii-ii-i-iv d) i-iii-ii-iv

(5) Physical and electrical specification is given in _____

a) architectural design b) logic design
c) circuit design d) layout design

(6) Gate minimization technique is used to simplify the logic.

a) true b) false
c) In the case of Silicon, even if the number of the gate is minimised, logic will not be simplified d) In the case of Ge, even if the number of the gate is minimised, logic will not be simplified

(7) _____ impurities are added to the wafer of the crystal.

a) n impurities
b) p impurities
c) silicon
d) crystal

(8) What kind of layer is provided upon which other layers may be deposited and patterned.

a) insulating
b) conducting
c) silicon
d) semiconducting

(9) The photoresist layer is exposed to _____

a) Visible light
b) Ultraviolet light
c) Infra red light
d) LED

(10) Electronics are characterized by _____

a) low cost
b) low weight and volume
c) reliability
d) low cost, low weight and volume, reliability

(11) nMOS devices are formed in _____

a) p-type substrate of high doping level
b) n-type substrate of low doping level
c) p-type substrate of moderate doping level
d) n-type substrate of high doping level

(12) Speed power product is measured as the product of _____

a) gate switching delay and gate power dissipation
b) gate switching delay and gate power absorption
c) gate switching delay and net gate power
d) gate power dissipation and absorption

(13) In depletion mode, source and drain are connected by _____

a) insulating channel
b) conducting channel
c) Vdd
d) Vss

(14) In enhancement mode, device is in _____ condition.

a) conducting
b) non conducting
c) partially conducting
d) insulating

(15) What is the condition for non conducting mode?

a) Vds lesser than Vgs
b) Vgs lesser than Vds
c) Vgs = Vds = 0
d) Vgs = Vds = Vs = 0

(16) MOS transistor structure is _____

a) symmetrical
b) non symmetrical
c) semi symmetrical
d) pseudo symmetrical

(17) Which is the commonly used bulk substrate in nMOS fabrication?

a) either bulk silicon or silicon-on-sapphire
b) silicon-di-oxide
c) aluminium
d) copper

(18) In diffusion process of nMOS, _____ impurity is desired.

a) n type
b) p type
c) np type
d) none of the mentioned

(19) Interconnection pattern is made on _____

a) polysilicon layer
b) silicon-di-oxide layer
c) metal layer
d) diffusion layer

(20) Which is used for the interconnection?

a) boron
b) oxygen
c) aluminium
d) silicon

(21) The FPGA refers to _____

a) First programmable Gate Array
b) Field Programmable Gate Array
c) First Program Gate Array
d) Field Program Gate Array

(22) In which design, all circuitry and all interconnections are designed?

a) full custom design
b) semi-custom design
c) gate array design
d) transistor design

(23) Which design contains only the interconnections designed?

a) full custom design
b) semi-custom design
c) gate array design
d) transistor design

(24) In which method regularity is used to reduce complexity?

a) random approach
b) hierarchical approach
c) algorithmic approach
d) semi-design approach

(25) Which design is faster?

a) full custom design
b) semi-custom design
c) gate array design
d) transistor design

(26) The set of design rules does not give

a) widths
b) spacing
c) colours
d) overlaps

(27) Which type of digital systems exhibit the necessity for the existence of at least one feedback path from output to input?

a) Combinational System
b) Sequential system
c) Both Combinational and Sequential
d) None of Combinational and Sequential

(28) The full form of VLSI is _____

a) Very Long Single Integration
b) Very Least Scale Integration
c) Very Large Scale Integration
d) Very Long Scale Integration

(29) In FPGA, vertical and horizontal directions are separated by _____

a) A line
b) A channel
c) A strobe
d) A flip-flop

(30) The complex programmable logic device contains several PLD blocks and _____

a) A language compiler
b) AND/OR arrays
c) Global interconnection matrix
d) Field-programmable switches

(31) The conductivity of the pure silicon is raised by:

a) Introducing Dopants (impurities)
b) Increasing Pressure
c) Decreasing Temperature
d) Deformation of Lattice

(32) The n-type semiconductor have _____ as majority carriers.

a) Holes
b) Negative ions
c) Electrons
d) Positive ions

(33) The logical low voltage (logic 0) or negative voltage on the gate of p-MOSFET forms:

a) Channel of negative carriers
b) Channel is not formed
c) Channel is clipped
d) Channel of positive carriers

(34) A bubble is present in the symbol of

a) NMOS
b) PMOS

c) CMOS
d) DMOS

(35) Which MOSFET is generally connected to the Vdd in a circuit?

a) PMOS
b) NMOS
c) CMOS
d) DMOS

(36) The principle of the MOSFET operation is:

a) Control the conduction of current between the source and the drain, using the potential difference applied at the gate voltage as a control variable
b) Control the current conduction between the source and the gate, using the electric field applied at the drain voltage as a control variable
c) Control the current conduction between the PN junction, using the electric field generated by the bias voltage as a control variable
d) Control the current conduction between the PN junctions, using the electric potential generated by the gate voltage as a control variable

(37) The conduction of current IDS depends on: i) Gate to source voltage ii) Drain to source voltage iii) Bulk to source voltage iv) Threshold voltage v) Dimensions of MOSFET

a) Only i
b) Only i, ii and iii
c) Only v
d) All of the mentioned

(38) What will be the effect on output voltage if the positions of n-MOS and p-MOS in CMOS inverter circuit are exchanged?

a) Output is same
b) Output is reversed
c) Output is always high
d) Output is always low

(39) In the CMOS inverter the output voltage is measured across:

a) Drain of n-MOS transistor and ground
b) Source of p-MOS transistor and ground
c) Source of n-MOS transistor and source of p-MOS transistor
d) Gate of p-MOS transistor and Gate of n-MOS transistor

(40) When the input of the CMOS inverter is equal to Inverter Threshold Voltage Vth, the transistors are operating in:

a) N-MOS is cutoff, p-MOS is in Saturation
b) P-MOS is cutoff, n-MOS is in Saturation
c) Both the transistors are in linear region
d) Both the transistors are in saturation region

(41) The electrical equivalent component for MOS structure is:

a) Resistor
b) Capacitor
c) Inductor
d) Switch

(42) In negative logic convention, the Boolean Logic '1' is equivalent to:

a) +VDD
b) 0 V
c) -VDD
d) None of the mentioned

(43) When both nMOS and pMOS transistors of CMOS logic design are in OFF condition, the output is:

a) 1 or Vdd or HIGH state
b) 0 or ground or LOW state
c) High impedance or floating(Z)
d) None of the mentioned

(44) When both nMOS and pMOS transistors of CMOS logic gates are ON, the output is:

a) 1 or Vdd or HIGH state
b) 0 or ground or LOW state
c) Crowbarred or Contention(X)
d) None of the mentioned

(45) If A and B are the inputs of a half adder, the sum is given by _____

a) A AND B
b) A OR B

c) A XOR B
d) A EX-NOR B

(46) If A and B are the inputs of a half adder, the carry is given by _____

a) A AND B
b) A OR B
c) A XOR B
d) A EX-NOR B

(47) How many AND, OR and EXOR gates are required for the configuration of full adder?

a) 1, 2, 2
b) 2, 1, 2
c) 3, 1, 2
d) 4, 0, 1

(48) Latch is a device with _____

a) One stable state
b) Two stable state
c) Three stable state
d) Infinite stable states

(49) How many types of latches are _____

a) 4
b) 3
c) 2
d) 5

(50) The full form of SR is _____

a) System rated
b) Set reset
c) Set ready
d) Set Rated

(51) When both inputs of SR latches are low, the latch _____

a) Q output goes high
b) Q' output goes high
c) It remains in its previously set or reset state
d) it goes to its next set or reset state

(52) CMOS technology is used in developing which of the following?

a) microprocessors
b) microcontrollers
c) digital logic circuits
d) all of the mentioned

(53) Oxidation process is carried out using _____

a) high purity oxygen
b) low purity oxygen
c) sulphur
d) nitrogen

(54) Photoresist layer is formed using _____

a) high sensitive polymer
b) light-sensitive polymer
c) polysilicon
d) silicon dioxide

(55) Few parts of photoresist layer is removed by using _____

a) acidic solution
b) neutral solution
c) pure water
d) diluted water

(56) P-well doping concentration and depth will affect the _____

a) threshold voltage
b) Vss
c) Vdd
d) Vgs

(57) Which statement is false concerning Moore's Law?

a) The term was named for Gordon Moore.
b) Gordon Moore was one of the founders of IBM.
c) In the 1960s the storage density of integrated circuits on a silicon chip doubled about every year.
d) Today, when we speak of Moore's Law we refer to the doubling of computer power every 18 months.

(58) What type of integration is chosen to fabricate Integrated Circuits like Counters, multiplexers and Adders?

a) Small Scale Integration (SSI)
b) Medium Scale Integration (MSI)

c) Large Scale Integration (LSI)
d) Very Large Scale Integration (VLSI)

(59) MOS transistors consist of which of the following?

a) semiconductor layer
b) metal layer
c) layer of silicon-di-oxide
d) all of the mentioned

(60) In MOS transistors _____ is not used for their gate.

a) metal
b) silicon-di-oxide
c) polysilicon
d) gallium